

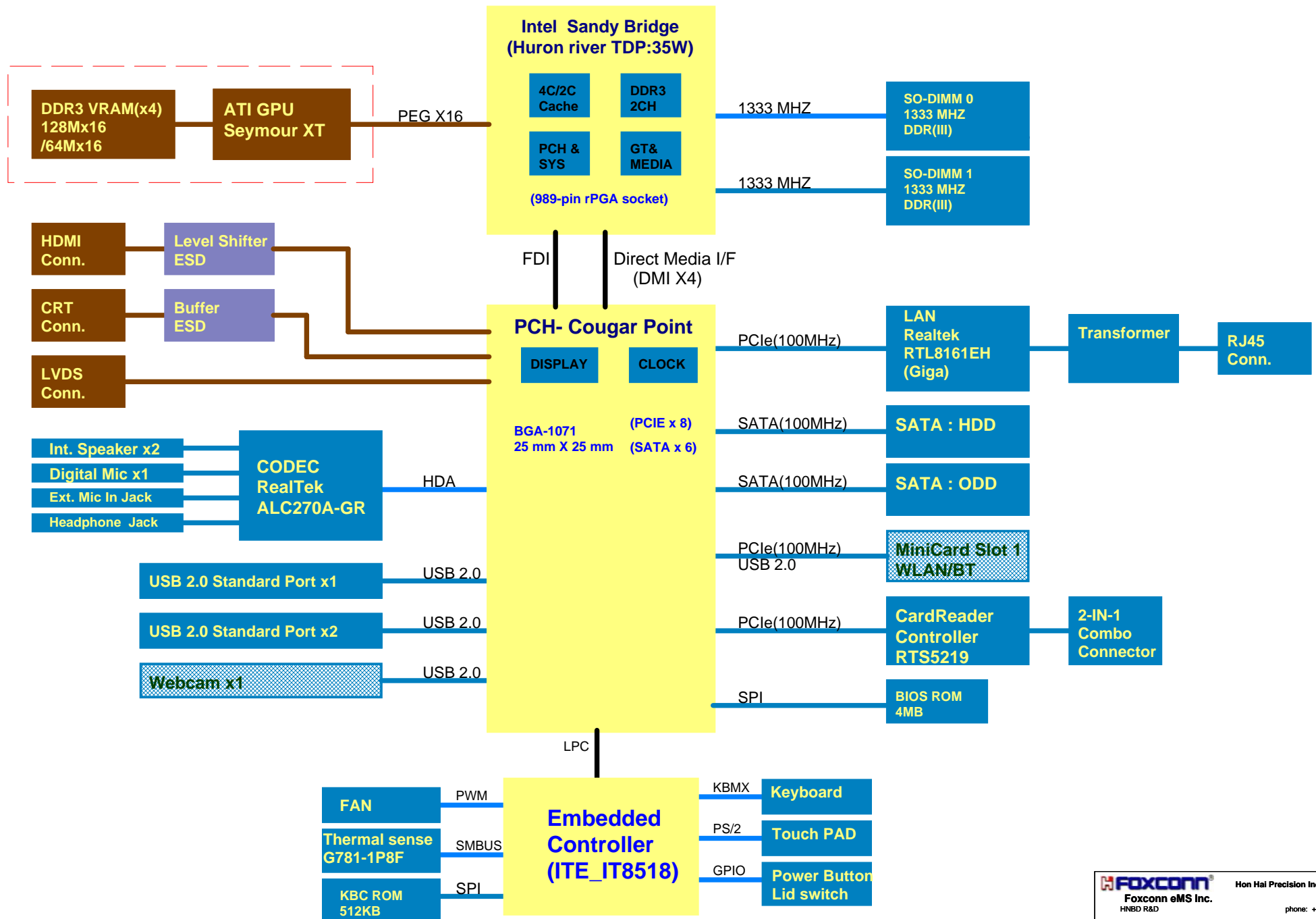
# PROJECT : CHICAGO (For Intel Huron River Platform)

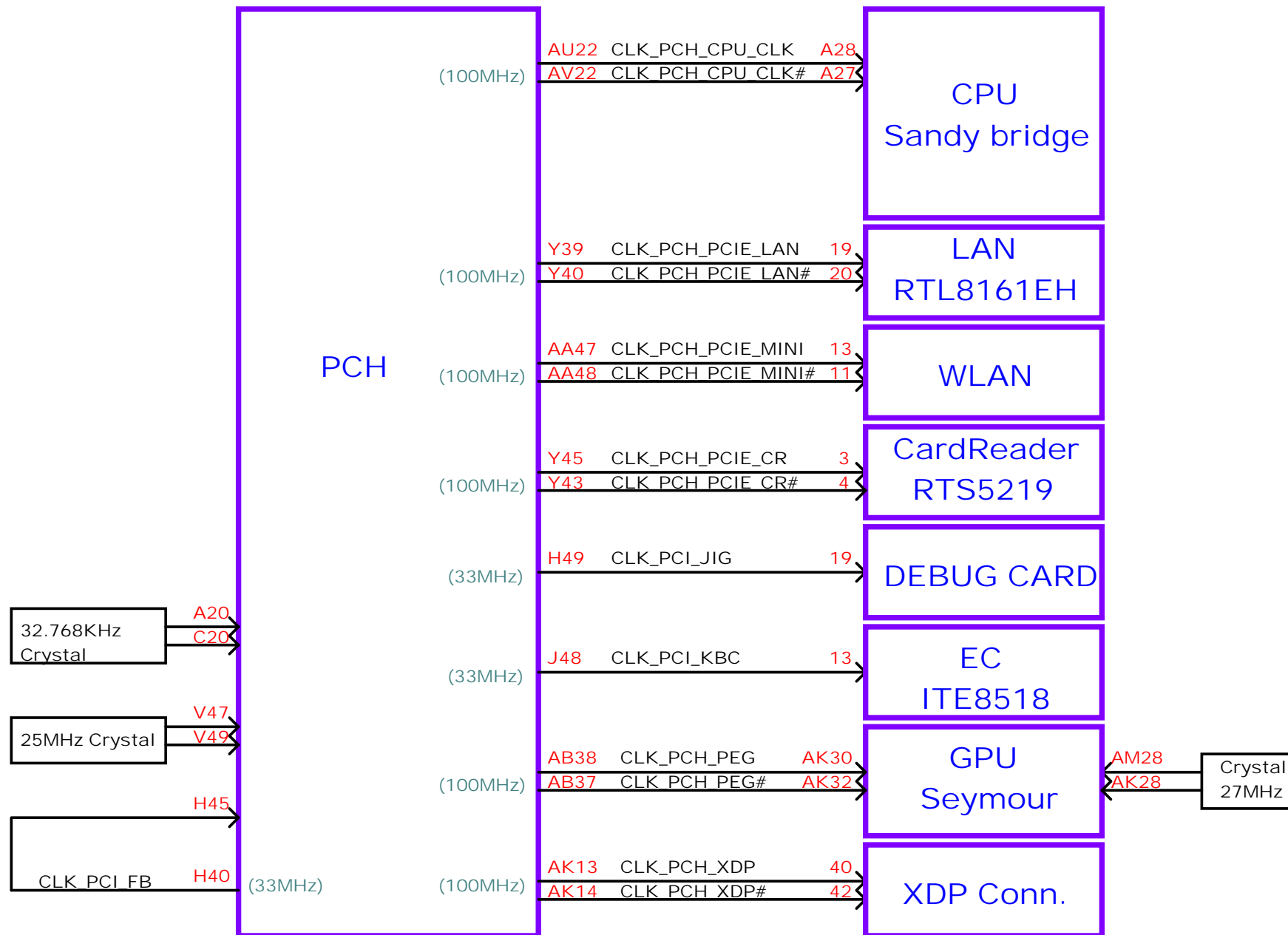
01 -- COVER SHEET  
 02 -- SYSTEM BLOCK DIAGRAM  
 03 -- CLOCK MAP  
 04 -- POWER SEQUENCY DIAGRAM  
 05 -- POWER MAP  
 06 -- SMBUS MAP  
 07 -- Blank  
 08 -- DCIN/BATT  
 09 -- PWR\_CHARGE  
 10 -- PWR\_5V/3.3V  
 11 -- PWR\_VCCP  
 12 -- PWR\_1.5V/0.75S  
 13 -- PWR\_VCORE  
 14 -- PWR\_OTHER  
 15 -- PWR\_ATVDD  
 16 -- PWR\_1.8VS  
 17 -- PWR\_VCCSA  
 18 -- Sandy Bridge(DMI,PEG,FDI)  
 19 -- Sandy Bridge(CLK,JTAG..)  
 20 -- Sandy Bridge(DDR3)  
 21 -- Sandy Bridge(PWR/GND)  
 22 -- Sandy Bridge(GRAPHIC PWR)

23 -- CougarPoint(HDA,SATA..)  
 24 -- CougarPoint(PCI-E,CLK..)  
 25 -- CougarPoint (DMI,FDI..)  
 26 -- CougarPoint(USB,GPIO..)  
 27 -- CougarPoint(PWR/GND)  
 28 -- CougarPoint(PWR,GND)  
 29 -- DDR3(SO-DIMM\_0&1)  
 30 -- VGA (PCI-E/STRAP) 1/3  
 31 -- VGA\_S3 (IO) 2/3  
 32 -- VGA\_S3 (DDR3) 3/3  
 33 -- VRAM (DDR3)  
 34 -- EC+KBC (IT8518) & ROM  
 35 -- Audio (CODEC\_ALC270A)  
 36 -- Audio (JACK+AMP+SPK+Mute)  
 37 -- LAN (RTL8161EH)  
 38 -- Mini PCIe & FAN  
 39 -- USBx2/USB DB/SATA CONN.  
 40 -- Card Reader(RTL5219-GR)  
 41 -- HDMI & CRT  
 42 -- LVDS & Webcam  
 43 -- Sequence circuit

P. Leader	Check by	Design by

 <b>Foxconn eMS Inc.</b> HNBD R&D		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111
Title		
Index Page		
Size	Document Number	Rev
Custom	CHICAGO	MV
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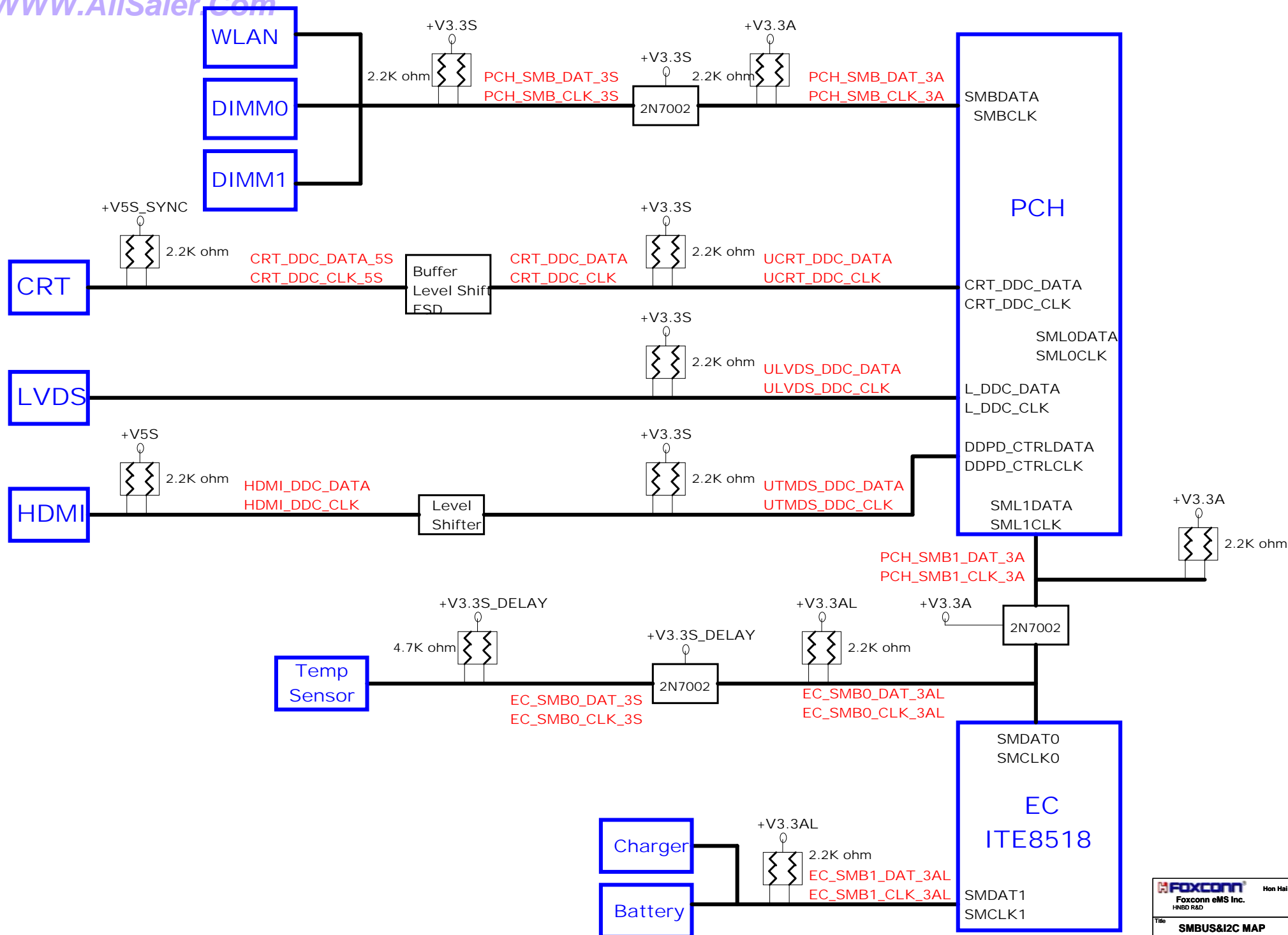


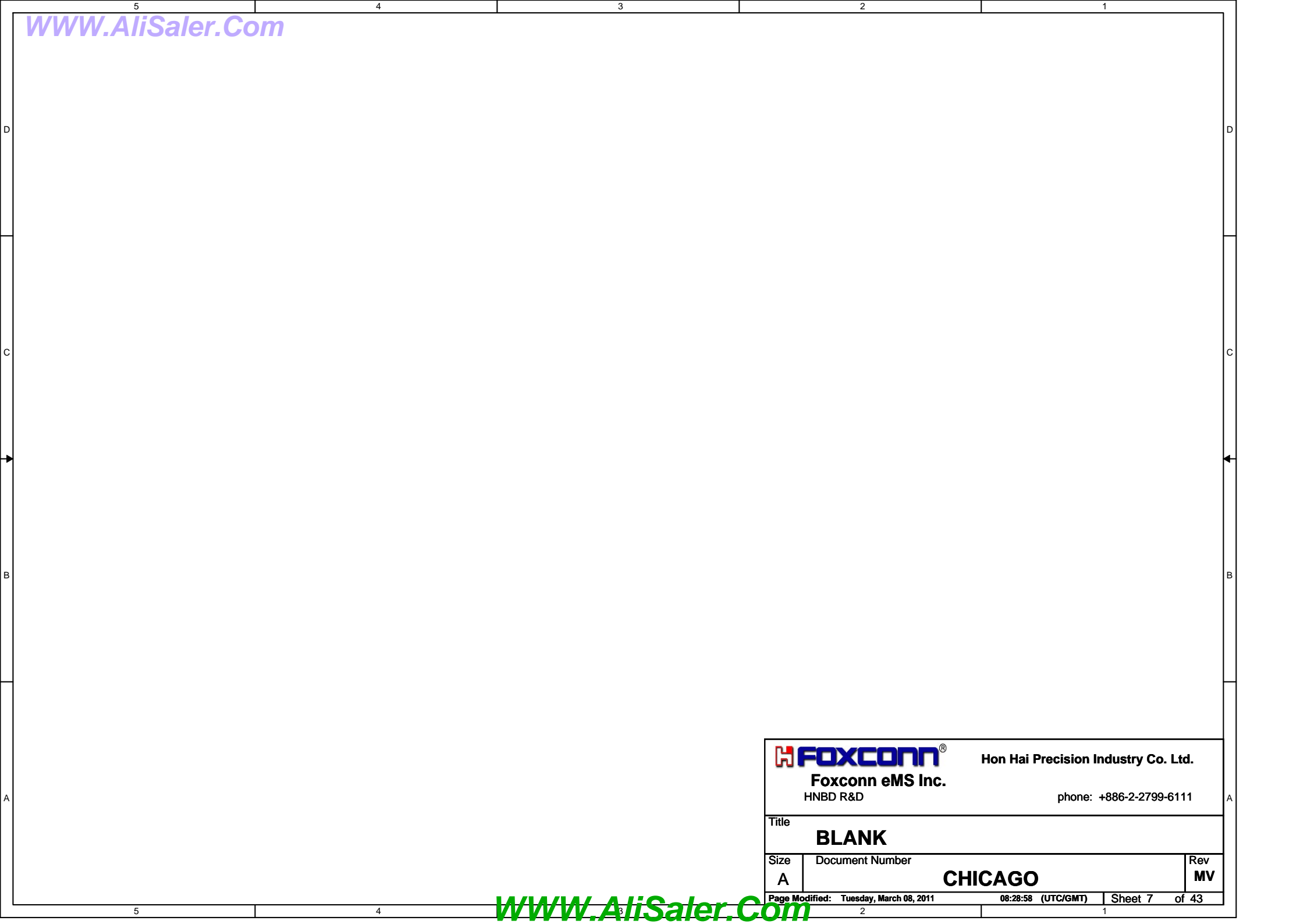




# POWER MAP





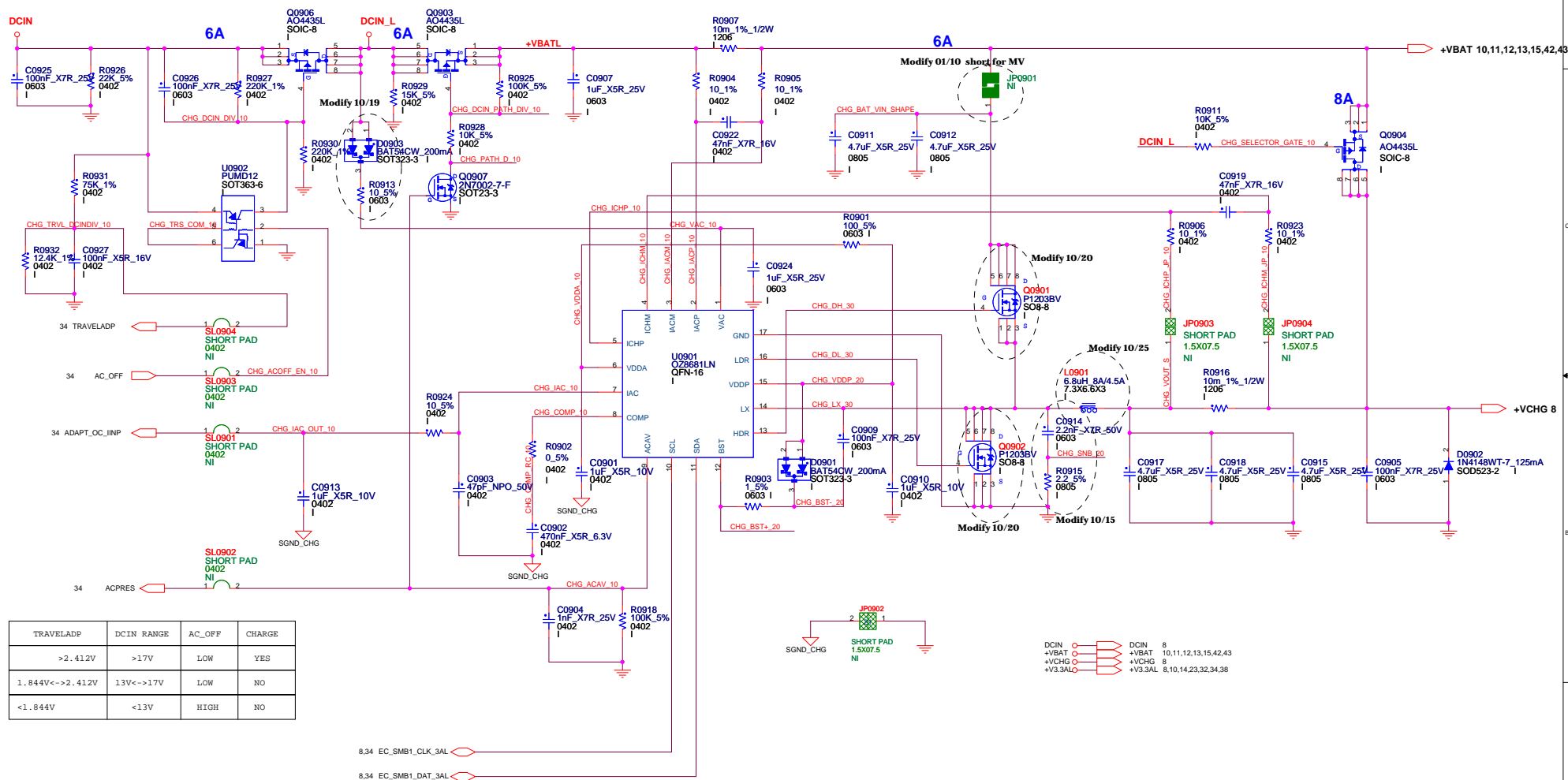


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HNBD R&D		phone: +886-2-2799-6111	
Title			
<b>BLANK</b>			
Size	Document Number		Rev
<b>A</b>	<b>CHICAGO</b>		<b>MV</b>
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## BATTERY CHARGER

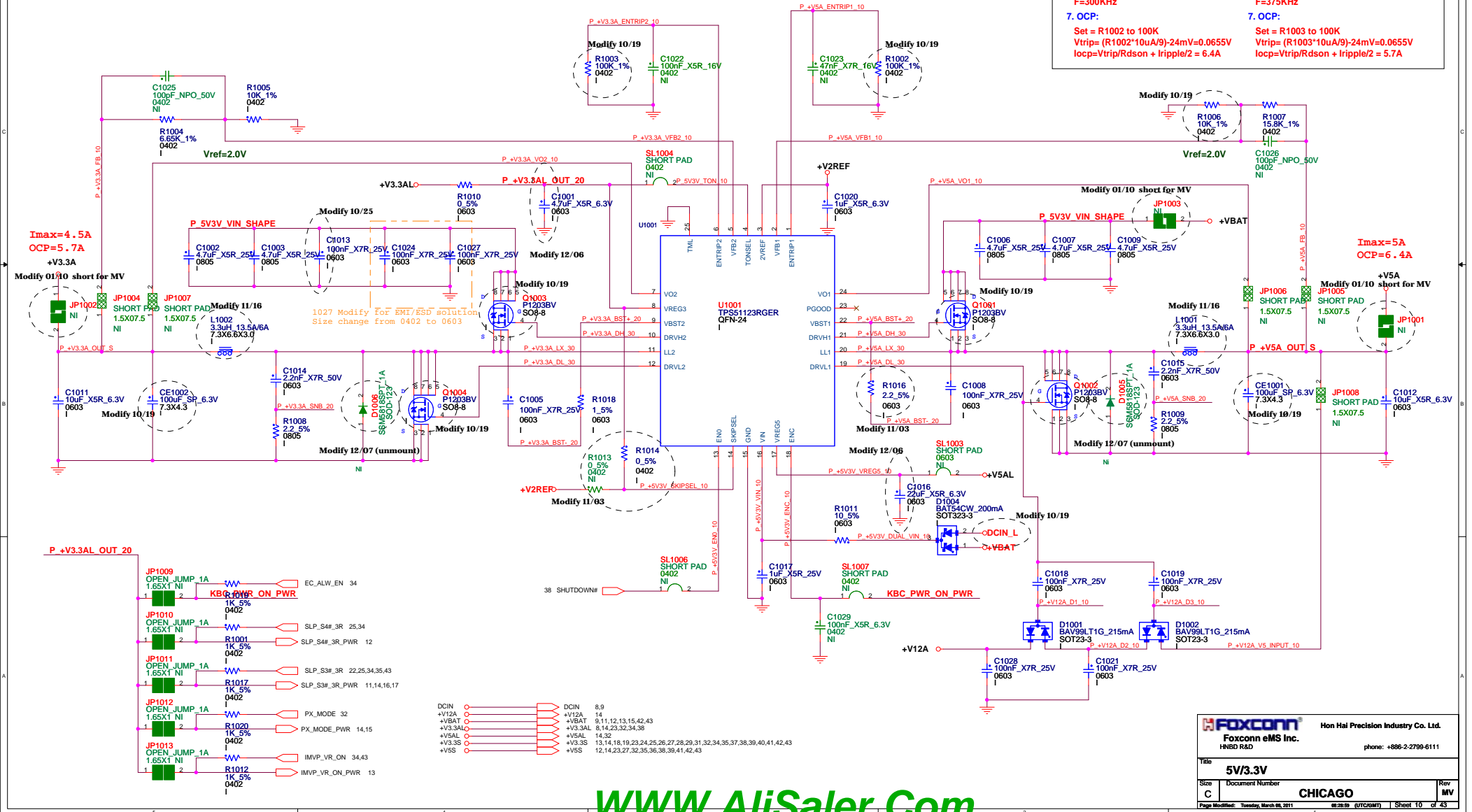


TRAVELADP	DCIN_RANGE	AC_OFF	CHARGE
>2.412V	>17V	LOW	YES
1.844V<->2.412V	13V<->17V	LOW	NO
<1.844V	<13V	HIGH	NO

# +V5A / +V3.3A POWER SUPPLY

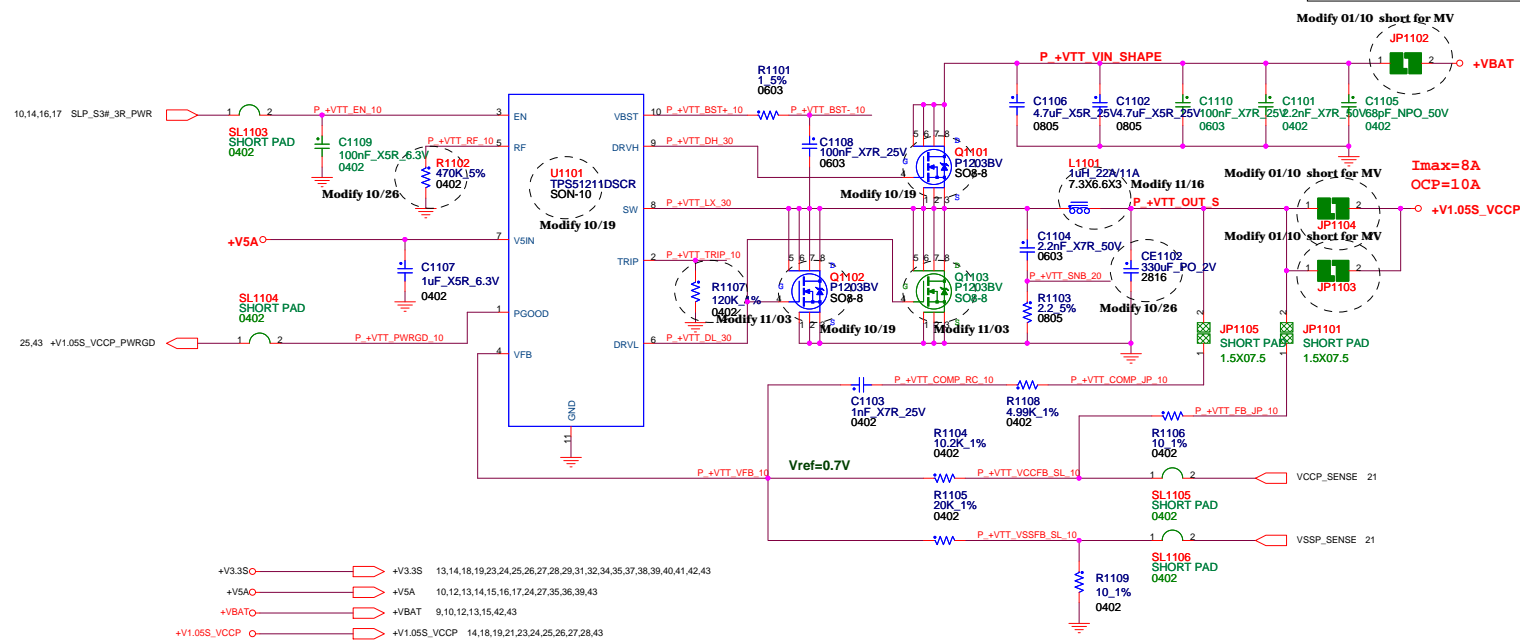
2010.1103.0

- |  |   |
|--|---|
| <p><b>+V5A:</b></p> <ol style="list-style-type: none"> <li>1. IP Current:<br/><math>I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 3.7A</math></li> <li>2. Ripple Current:<br/><math>I_{rip} = 3.72A</math></li> <li>3. Ripple Voltage:<br/>ESR/1=15mohm<br/>Vrip=55.8mV</li> <li>4. Inductor Spec:<br/>Isat=13.5A<br/>Idc=6A<br/>DCR=30mohm</li> <li>5. MOSFET Spec:<br/>H-side MOSFET: IRF8707PBF<br/>Rds(ON)=17.5mohm (Vgs=4.5 V)<br/>I cont = 11A (T=25 °C)<br/>I peak = 88A (Pause =10 us)</li> <li>6. Frequency:<br/>F=300KHz</li> <li>7. OCP:<br/>Set = R1002 to 100K<br/>Vtrip= (R1002*10uA/9)-24mV=0.0655V<br/>Iocp=Vtrip/Rdson + Iripple/2 = 6.4A</li> </ol> | <p><b>+V3.3A:</b></p> <ol style="list-style-type: none"> <li>1. IP Current:<br/><math>I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.2A</math></li> <li>2. Ripple Current:<br/><math>I_{rip} = 2.21A</math></li> <li>3. Ripple Voltage:<br/>ESR/1=15mohm<br/>Vrip=33.15mV</li> <li>4. Inductor Spec:<br/>Isat=13.5A<br/>Idc=6A<br/>DCR=30mohm</li> <li>5. MOSFET Spec:<br/>L-side MOSFET: IRF8707PBF<br/>Rds(ON)=17.5mohm (Vgs=4.5 V)<br/>I cont = 11A (T=25 °C)<br/>I peak = 88A (Pause =10 us)</li> <li>6. Frequency:<br/>F=375KHz</li> <li>7. OCP:<br/>Set = R1003 to 100K<br/>Vtrip= (R1003*10uA/9)-24mV=0.0655V<br/>Iocp=Vtrip/Rdson + Iripple/2 = 5.7A</li> </ol> |
|--|---|

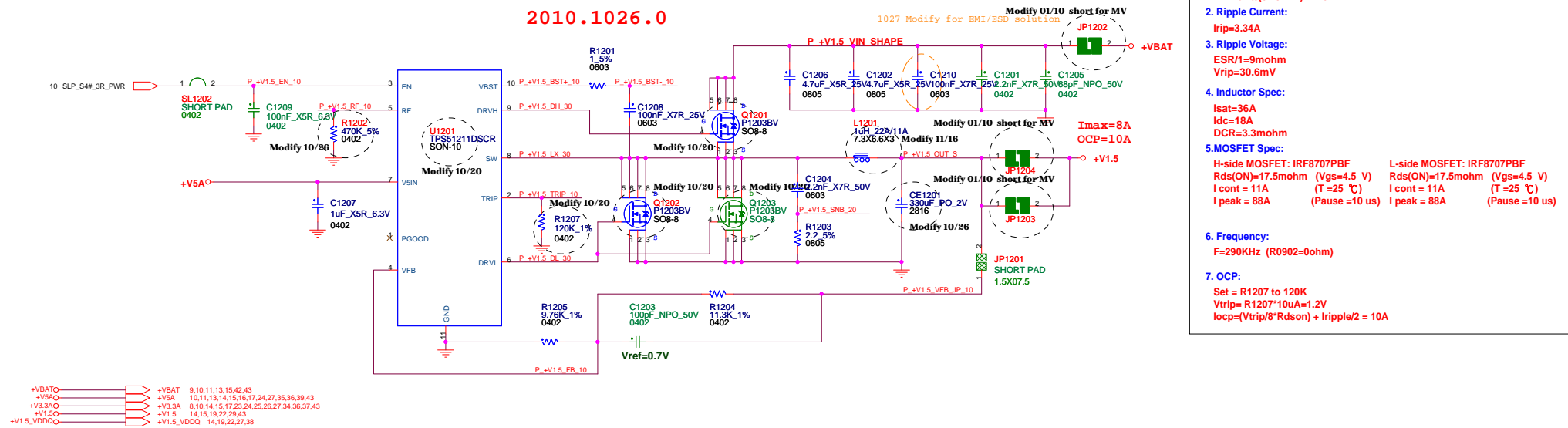


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- |  |   |                                     |  |
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| Title<br><div style="border: 1px solid black; padding: 5px; text-align: center;"> <b>+VTT</b> </div> |   |                                     |  |
| Size<br>C  | Document Number<br><div style="border: 1px solid black; padding: 5px; text-align: center;"> <b>CHICAGO</b> </div> | Rev<br>MV                           |  |
| Page Modified: Tuesday, March 08, 2011 (08:28:59 (UTC+GMT)) Sheet 11 of 43                           |   |                                     |  |

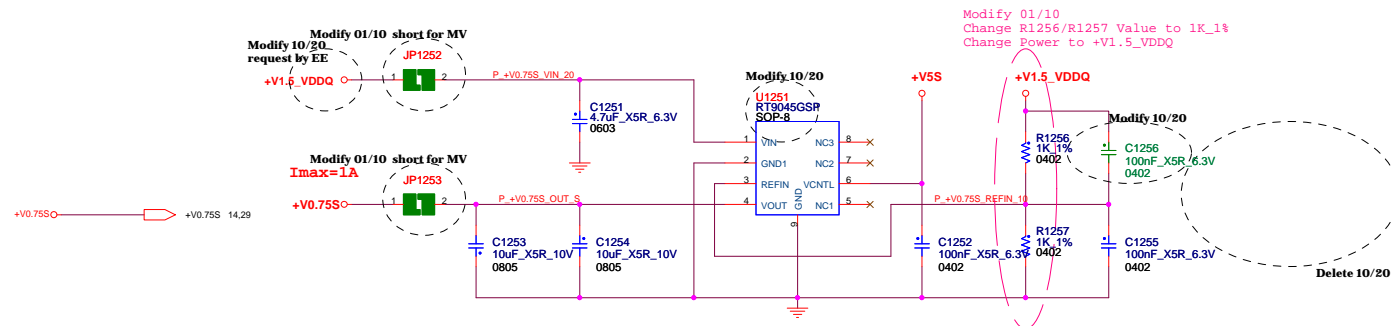


## 2010.1026.0



## +V0.75S POWER SUPPLY

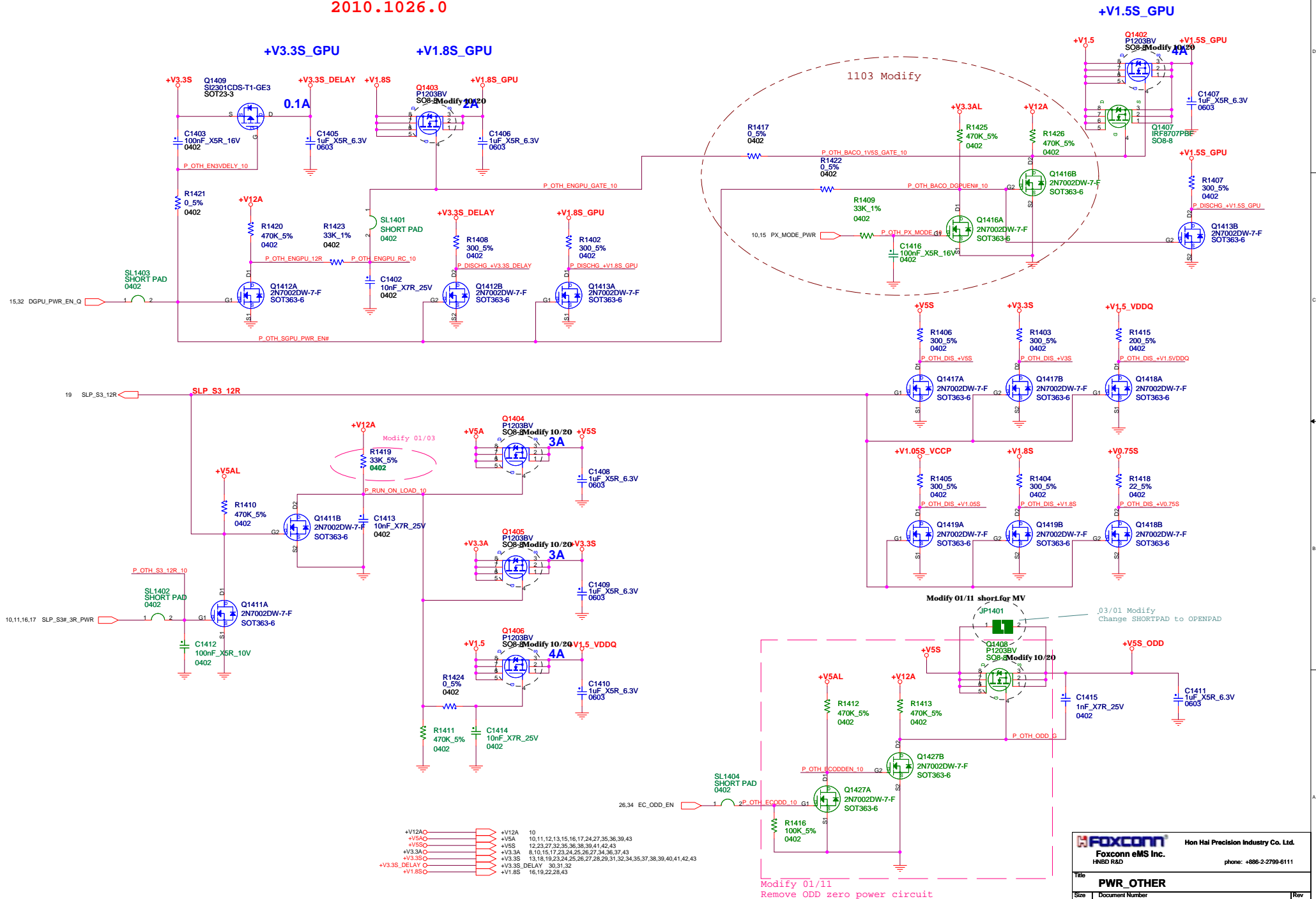
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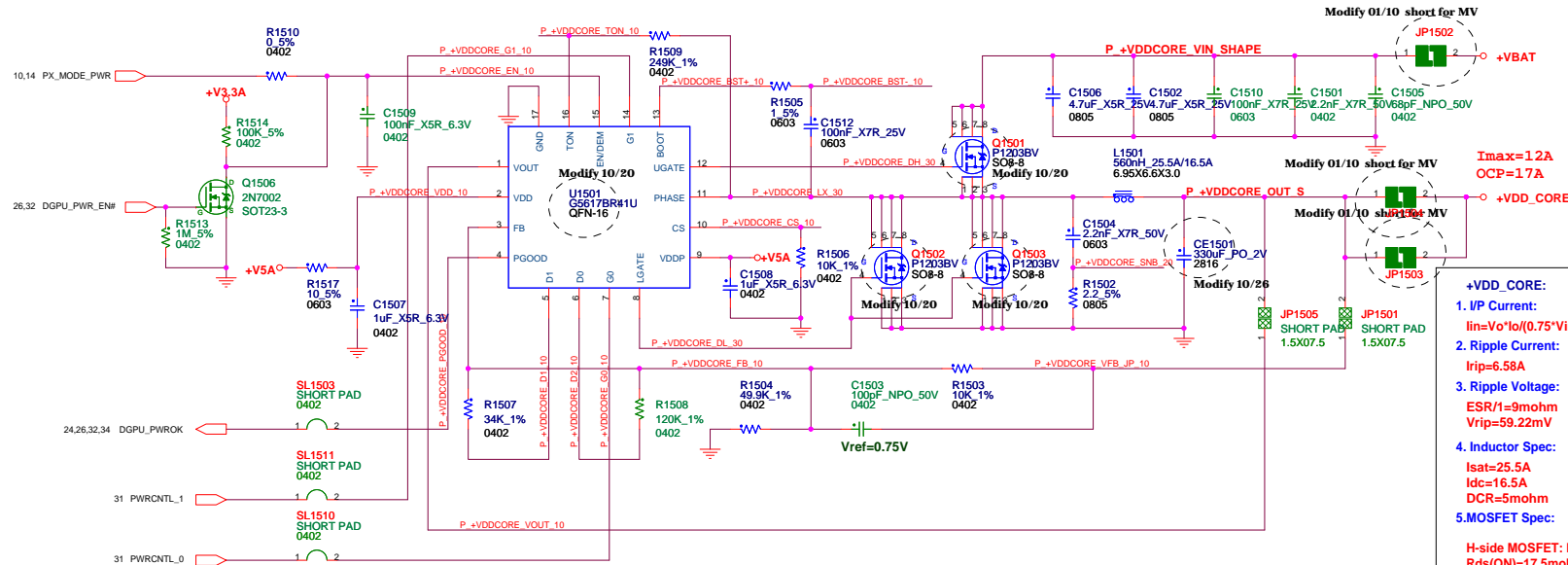
**WWW.AliSaler.Com**



2010.1026.0



2010.1026.0

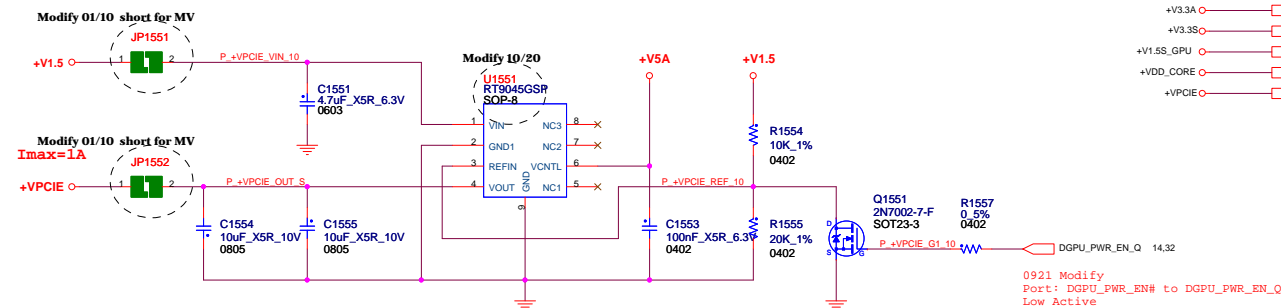


PWRCNTL_1	PWRCNTL_0	VDD_CORE
0	---	1.121V
---	---	---
1	---	0.9V
---	---	---

**+VDD\_CORE:**

1. VP Current:  
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.48A$
2. Ripple Current:  
 $I_{rip} = 6.58A$
3. Ripple Voltage:  
 $ESR / I = 9m\Omega$   
 $V_{rip} = 59.22mV$
4. Inductor Spec:  
 $I_{sat} = 25.5A$   
 $I_{dc} = 16.5A$   
 $DCR = 5m\Omega$
5. MOSFET Spec:
- |  |  |
|--|--|
| H-side MOSFET: IRF8707PBF                      | L-side MOSFET: IRF8707PBF                      |
| $R_{ds(ON)} = 17.5m\Omega$ ( $V_{gs} = 4.5V$ ) | $R_{ds(ON)} = 17.5m\Omega$ ( $V_{gs} = 4.5V$ ) |
| $I_{cont} = 11A$ ( $T = 25^\circ C$ )          | $I_{cont} = 11A$ ( $T = 25^\circ C$ )          |
| $I_{peak} = 88A$ (Pause = 10 us)               | $I_{peak} = 88A$ (Pause = 10 us)               |
6. Frequency:  
 $TON = 9.6P \cdot R_{1509} \cdot (VOUT + 0.1) / (VIN - 0.3) + 50ns = 206ns$   
 $F = VOUT / (VIN \cdot TON) = 286KHz$
7. OCP:
- Set =  $R_{1506} \cdot 10K$   
 $V_{trip} = R_{1206} \cdot 10uA = 0.1V$   
 $I_{ocp} = (V_{trip} / R_{ds(on)}) + I_{ripple} / 2 = 17A$

## 2010.1020.0 +VPCIE POWER SUPPLY



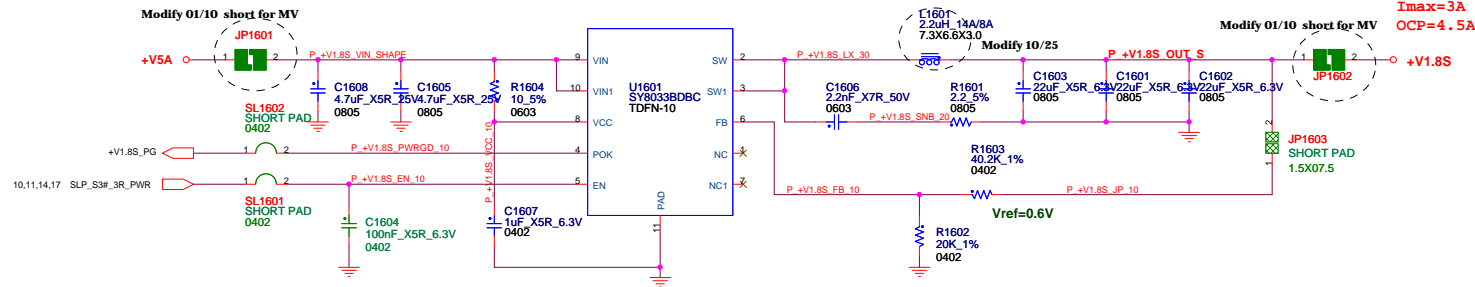
+VBAT		+VBAT	9,10,11,12,13,42,43
+V5A		+V5A	10,11,12,13,14,16,17,24,27,35,36,39,43
+V3.3A		+V3.3A	8,10,14,17,23,24,25,26,27,34,36,37,43
+V3.3S		+V3.3S	13,14,18,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1_SS_GPU		+V1_SS_GPU	14,30,32,33,43
+VDD_CORE		+VDD_CORE	32,43
+VPCIE		+VPCIE	30,31,32,43

```
0921 Modify
Port: DGPU_PWR_EN# to DGPU_PWR_EN_Q
Low Active
```

# +V1.8S POWER SUPPLY

2010.1025.0

- +V1.8S:**
- I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.44A$
  - Ripple Current:**  
 $I_{rip} = 0.53A$
  - Ripple Voltage:**  
 $ESR/3 = 3.3mohm$   
 $V_{rip} = 1.75mV$
  - Inductor Spec:**  
 $I_{sat} = 14A$   
 $I_{dc} = 8A$   
 $DCR = 20mohm$
  - MOSFET Spec:**  
H-side P-MOSFET:  $R_{ds(ON)} = 110mohm$  ( $V_{gs} = 4.5V$ )  
L-side N-MOSFET:  $R_{ds(ON)} = 75mohm$  ( $V_{gs} = 4.5V$ )
  - Frequency:**  
 $F = 1MHz$  (min=800KHz, max=1.2MHz)
  - OCP:**  
 $I_{ocp} = 4A(min)/4.5A(typ)/5A(max)$

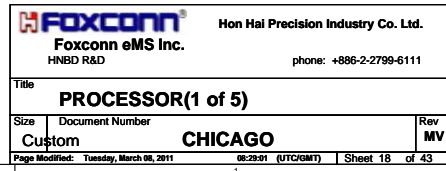


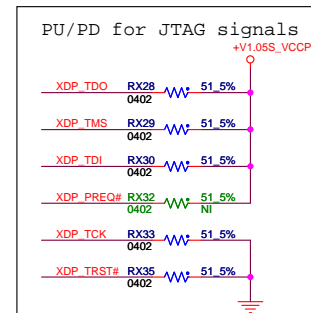


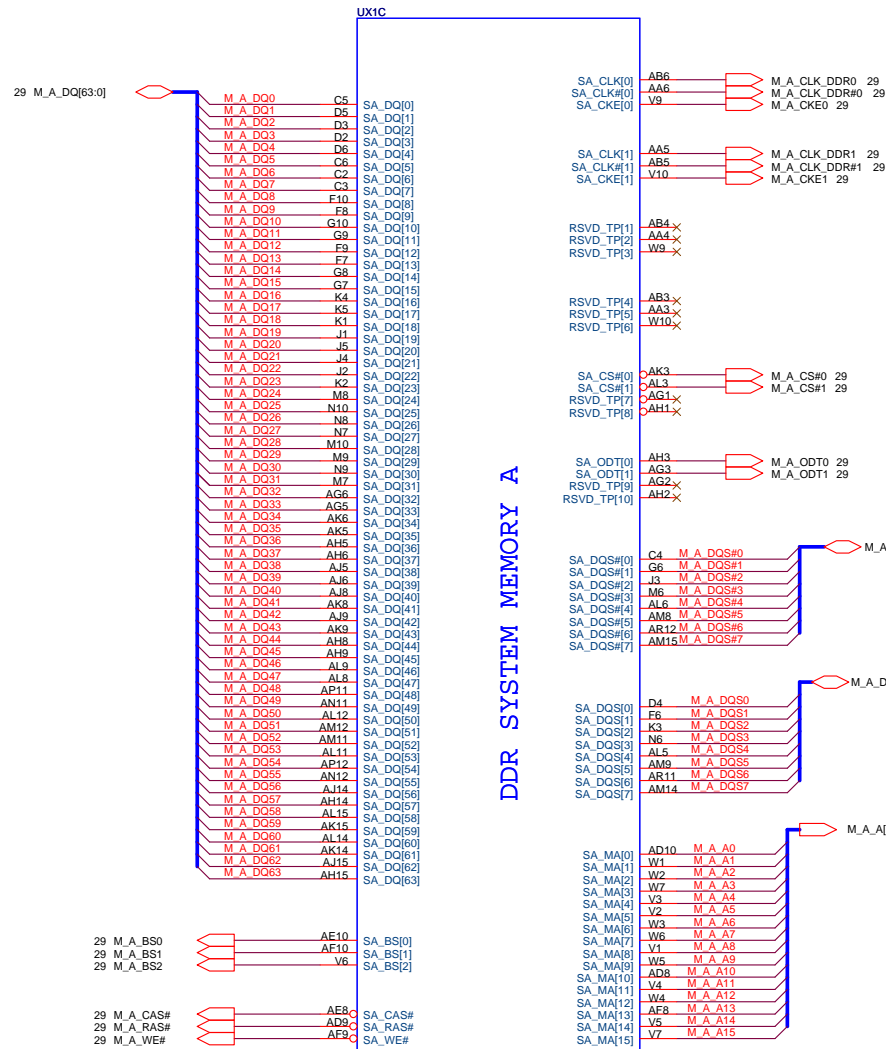
2010.1026.0



<b>VCCSA_SEL</b>	<b>+VCCSA</b>
H	0.80V
L	0.90V





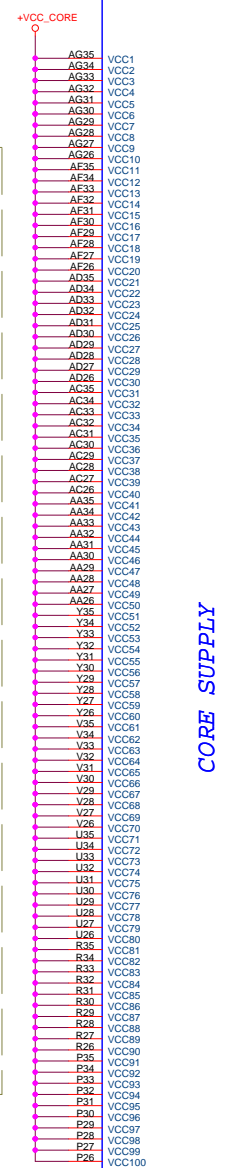
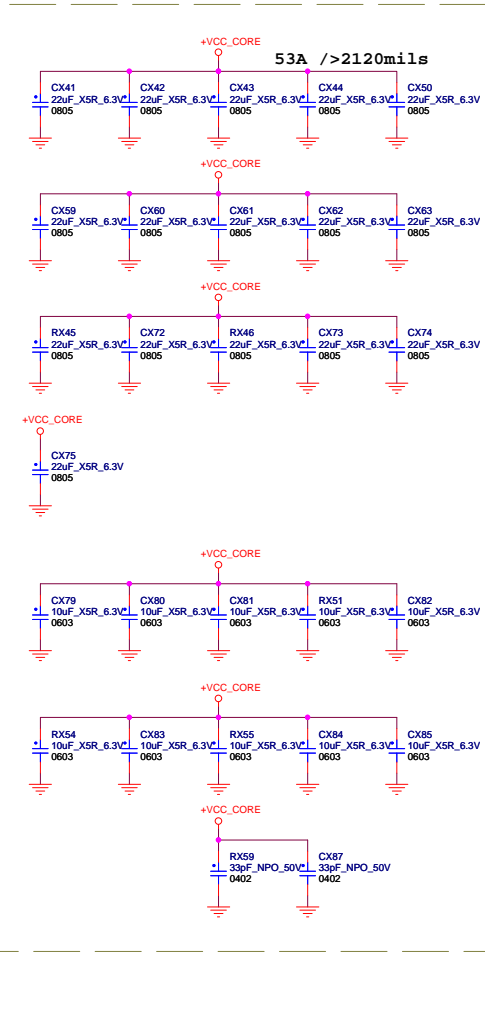


DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

+V1.05S\_VCCP 11,14,18,19,23,24,25,26,27,28,43  
+VCC\_CORE 13,18,43

FOR VCC:  
4x 330  $\mu$ F Bottom Edge,  
10x 0603 10  $\mu$ F Bottom Cavity,  
8x 0805 22  $\mu$ F Top Cavity,  
8x 0805 22  $\mu$ F Top Edge,



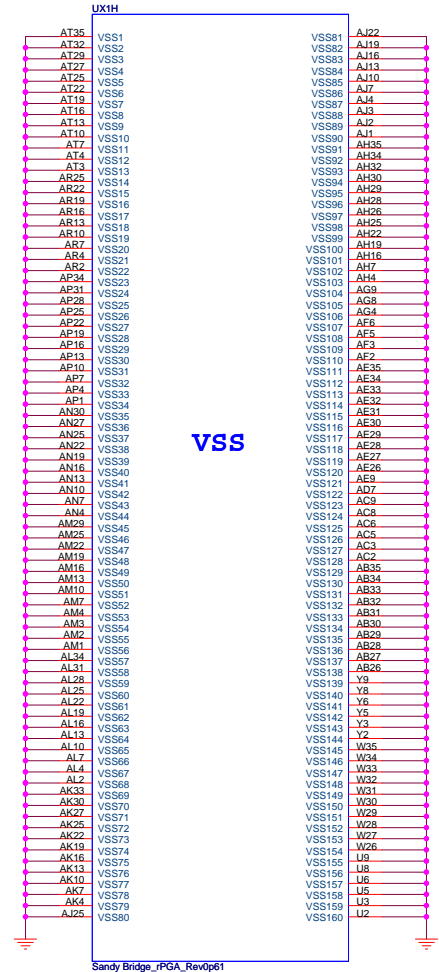
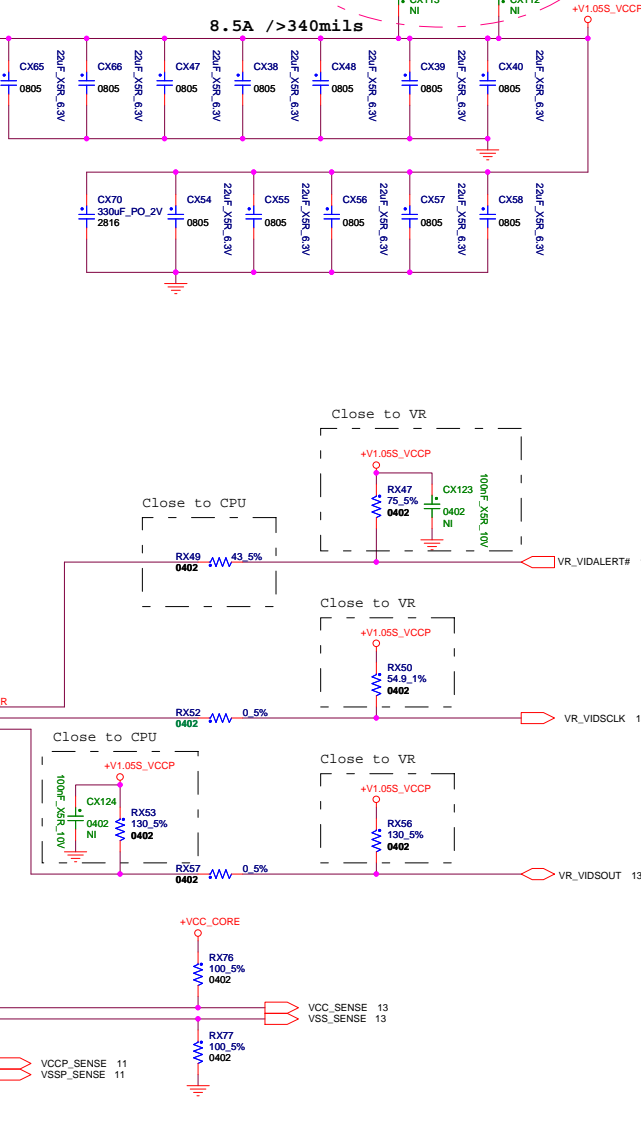
## POWER

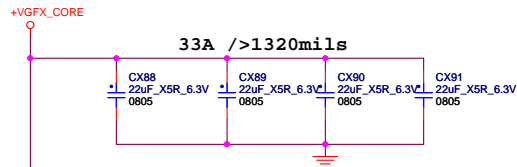
## PEG AND DDR

## CORE SUPPLY

## SENSE LINES

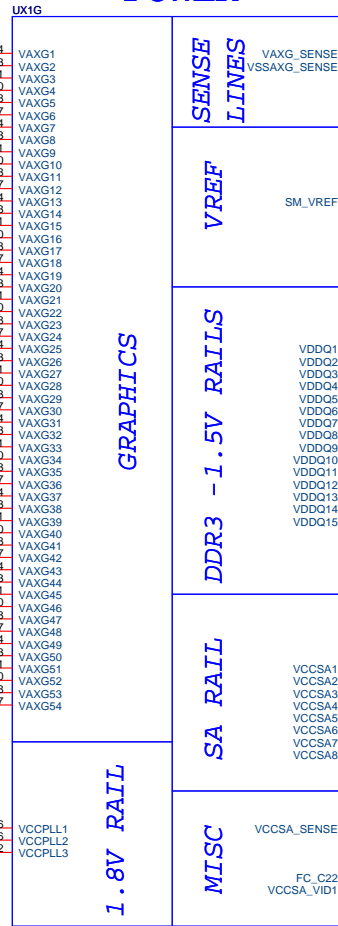
FOR VCCIO:  
2x 330  $\mu$ F,  
5x 0805 22  $\mu$ F Bottom Cavity,  
7x 0805 22  $\mu$ F Top Cavity,



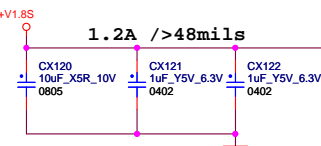


FOR VAXG:  
2x 330  $\mu$ F Bottom Edge,  
4x 0805 22  $\mu$ F Top & Bottom Cavity,  
8x 0805 22  $\mu$ F Top & Bottom Edge,

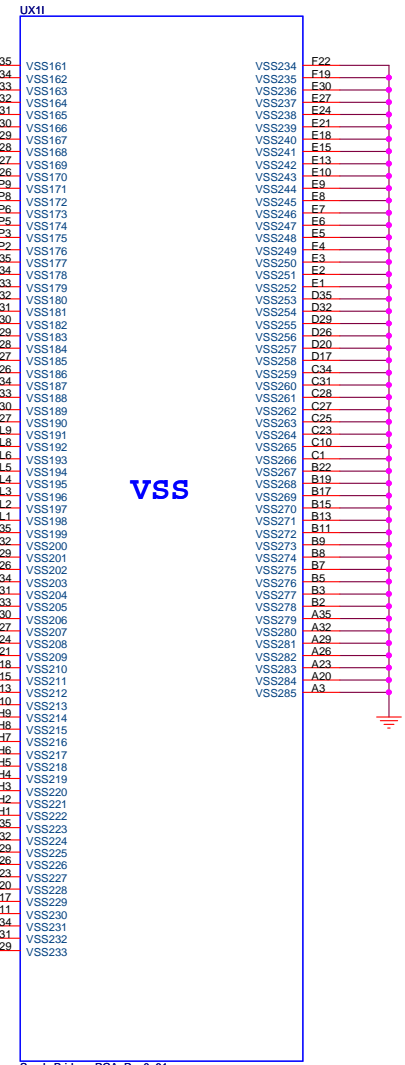
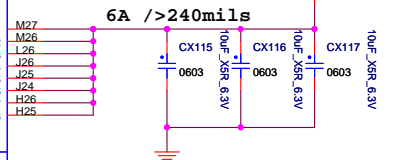
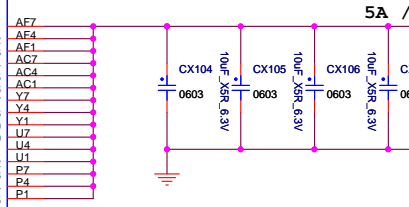
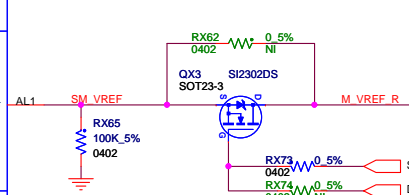
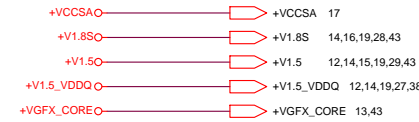
## POWER



Sandy Bridge\_rPGA\_Rev0p61

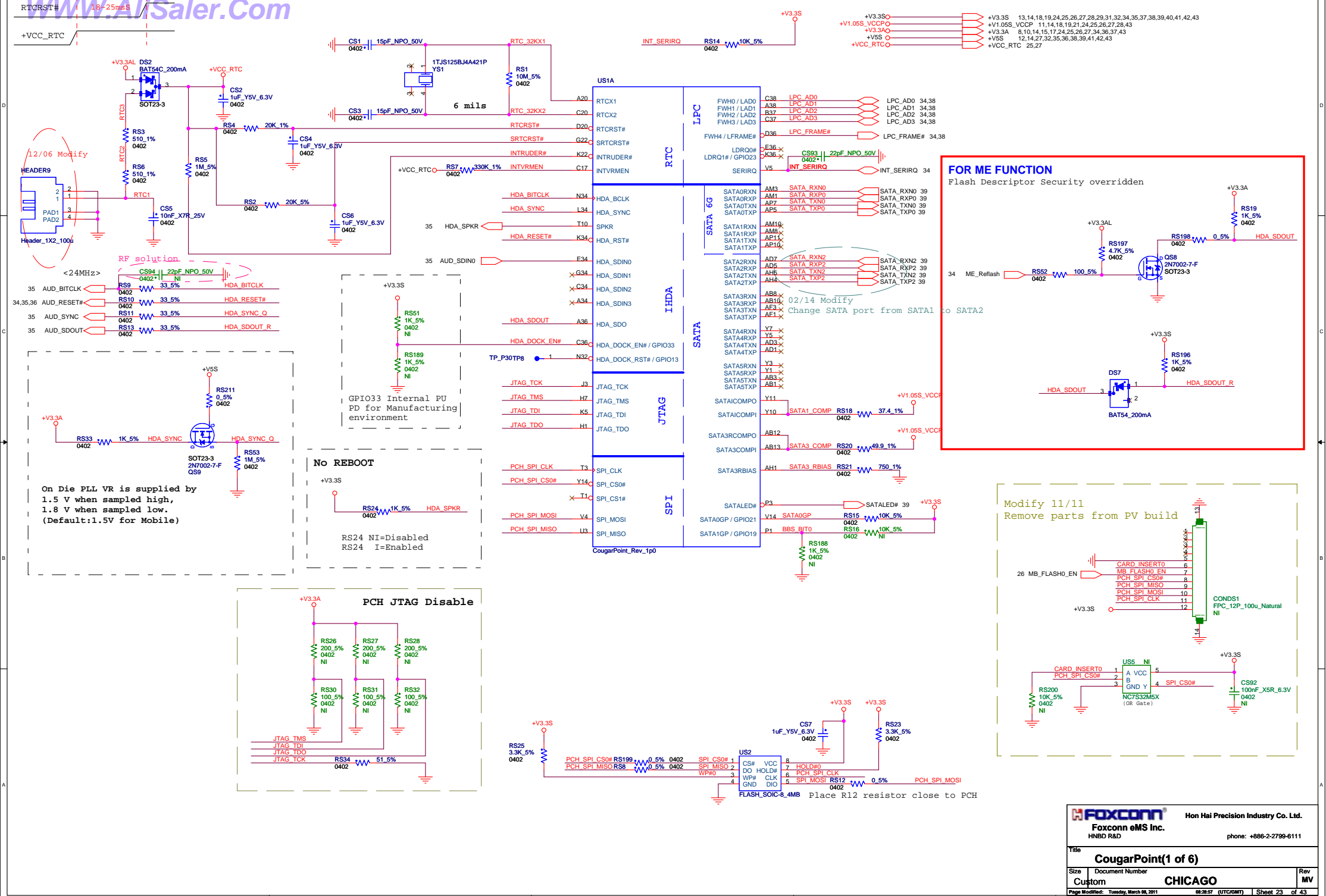


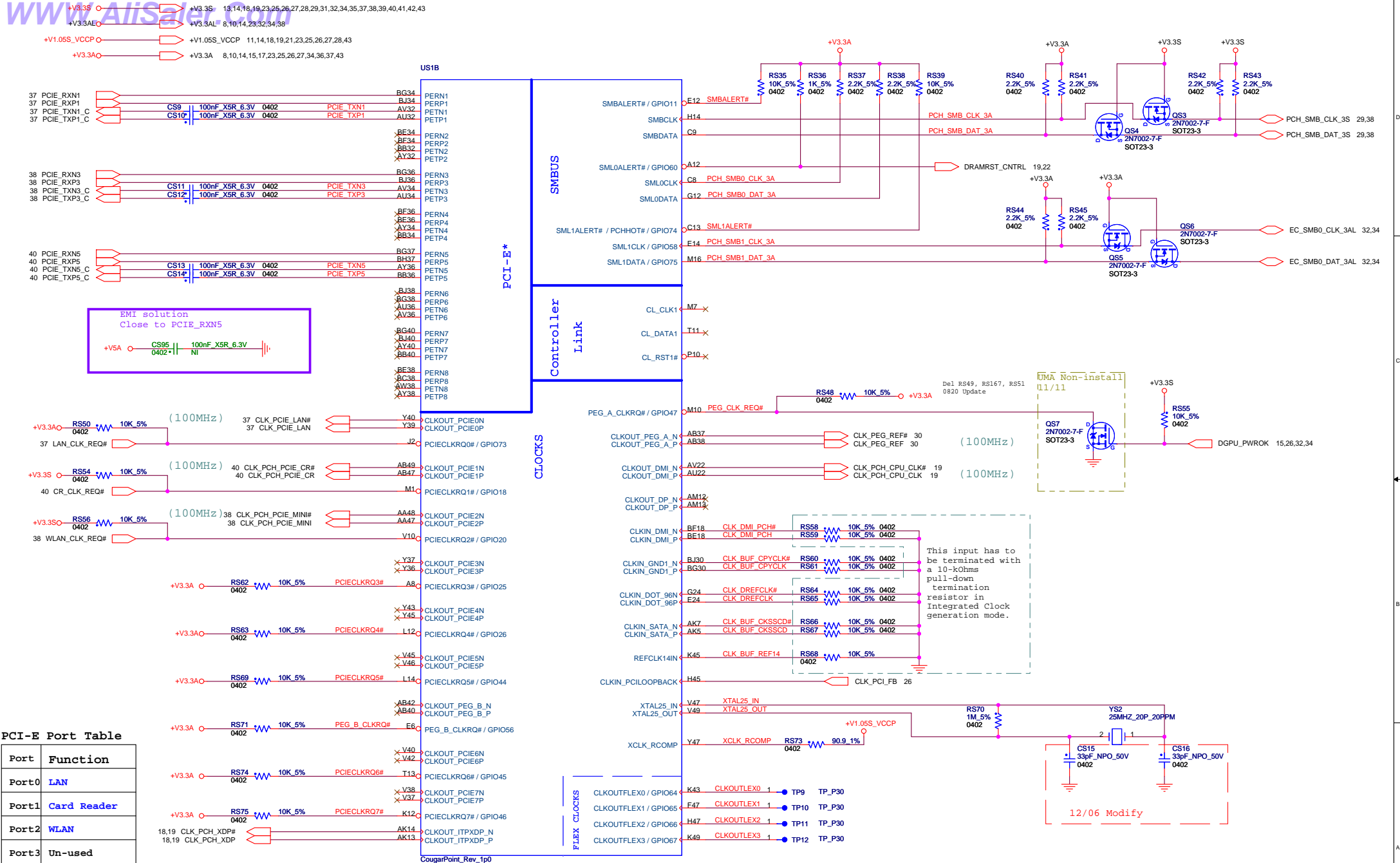
FOR VCCPLL:  
1x 330  $\mu$ F Bottom Edge,  
2x 0402 1  $\mu$ F Bottom Edge,  
1x 0805 10  $\mu$ F Bottom Edge,



Sandy Bridge\_rPGA\_Rev0p61









US1C

US1D

US1E

US1F

US1G

US1H

US1I

US1J

US1K

US1L

US1M

US1N

US1O

US1P

US1Q

US1R

US1S

US1T

US1U

US1V

US1W

US1X

US1Y

US1Z

US1A

US1B

US1C

US1D

US1E

US1F

US1G

US1H

US1I

US1J

US1K

US1L

US1M

US1N

US1O

US1P

US1Q

US1R

US1S

US1T

US1U

US1V

US1W

US1X

US1Y

US1Z

US1A

US1B

US1C

US1D

US1E

US1F

US1G

US1H

US1I

US1J

US1K

US1L

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US1P

US1Q

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US1S

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US1U

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US1B

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US1E

US1F

US1G

US1H

US1I

US1J

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US1O

US1P

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US1S

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US1W

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US1Z

US1A

US1B

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US1D

US1E

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US1H

US1I

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US1K

US1L

US1M

US1N

US1O

US1P

US1Q

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US1T

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US1V

US1W

US1X

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US1V

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US1Y

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US1B

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US1E

US1F

US1G

US1H

US1I

US1J

US1K

US1L

US1M

US1N

US1O

US1P

US1Q

US1R

US1S

US1T

US1U

US1V

US1W

US1X

Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

US1E

TP1  
TP2  
TP3  
TP4  
TP5  
TP6  
TP7  
TP8  
TP9  
TP10  
TP11  
TP12  
TP13  
TP14  
TP15  
TP16  
TP17  
TP18  
TP19  
TP20

TP21  
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TP23  
TP24

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TP27  
TP28  
TP29  
TP30  
TP31  
TP32  
TP33  
TP34  
TP35  
TP36  
TP37  
TP38  
TP39  
TP40

RSVD

PCI

USB

CougarPoint\_Rev\_1p0

Modify CS102/CS103 to non-stuff on 01/11

02/24 Modify same as the PV build

USB PORT	Function	OC#
PORT-0	USB Port	OC0#
PORT-1	USB Port	
PORT-2	USB Port	
PORT-3	NC	OC1#
PORT-4	NC	
PORT-5	NC	
PORT-6	NC	
PORT-7	NC	
PORT-8	NC	
PORT-9	NC	
PORT-10	Camera	
PORT-11	WLAN/BT	
PORT-12	NC	
PORT-13	NC	

US1F

GPIO

NCTF

CougarPoint\_Rev\_1p0

PLL ON DIE VR ENABLE		
GP28	0	disable
	1	Enable(Default)

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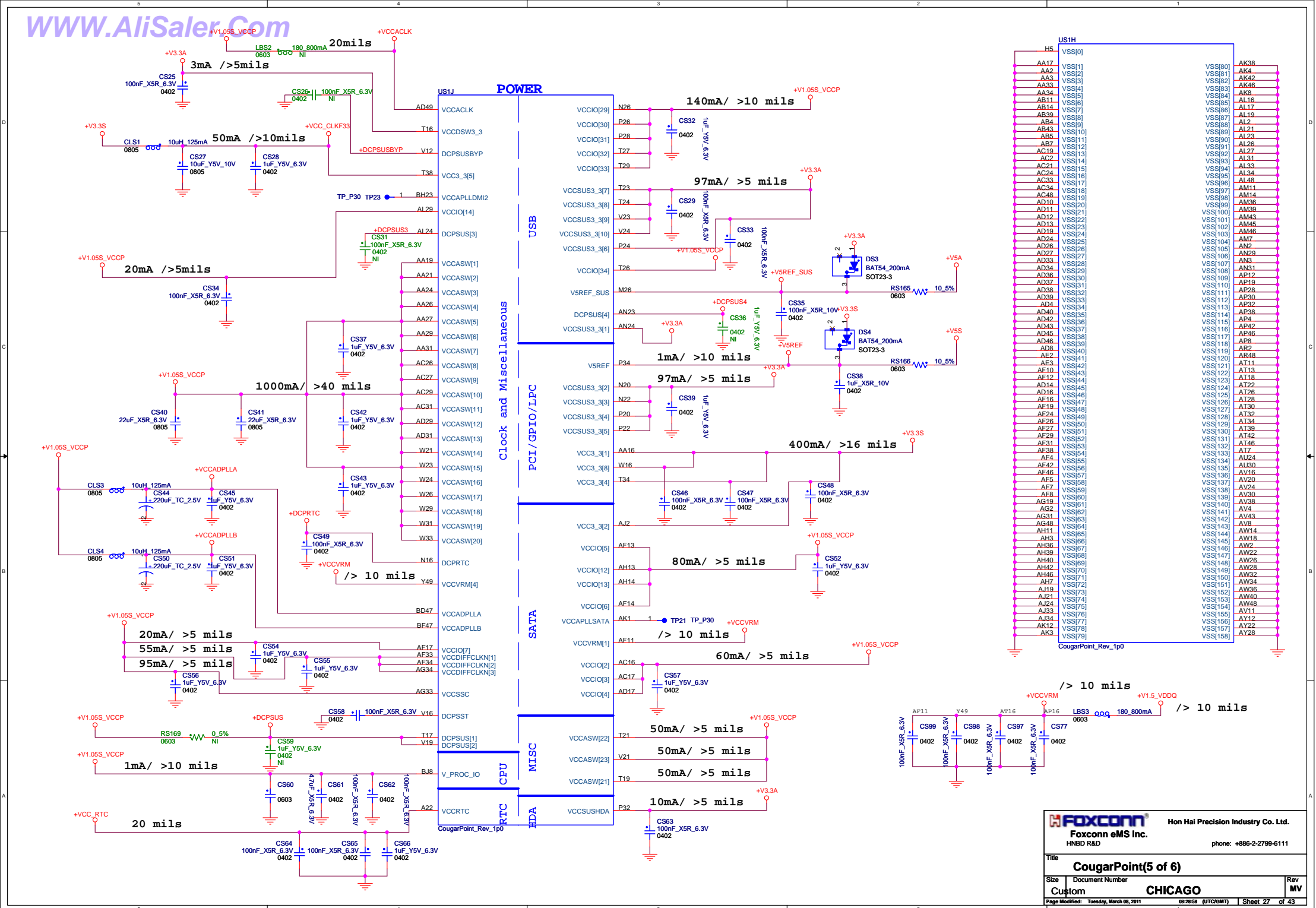
Title: **CougarPoint(4 of 6)**

Size: Document Number

Custom: **CHICAGO**

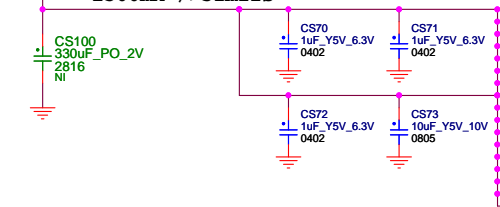
Rev: **MV**

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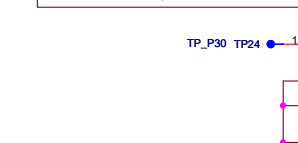


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AY42	VSS[160]	VSS[260]	K18
AY46	VSS[161]	VSS[261]	K26
AY8	VSS[162]	VSS[262]	K39
B11	VSS[163]	VSS[263]	K46
B15	VSS[164]	VSS[264]	K7
B19	VSS[165]	VSS[265]	L18
B23	VSS[166]	VSS[266]	L2
B27	VSS[167]	VSS[267]	L20
B31	VSS[168]	VSS[268]	L26
B35	VSS[169]	VSS[269]	L28
B39	VSS[170]	VSS[270]	L36
B7	VSS[171]	VSS[271]	L48
F45	VSS[172]	VSS[272]	M12
BB12	VSS[173]	VSS[273]	P16
BB16	VSS[174]	VSS[274]	M18
BB20	VSS[175]	VSS[275]	M22
BB22	VSS[176]	VSS[276]	M24
BB24	VSS[177]	VSS[277]	M32
BB28	VSS[178]	VSS[278]	M34
BB30	VSS[179]	VSS[279]	M36
BB38	VSS[180]	VSS[280]	M4
BB4	VSS[181]	VSS[281]	M42
BB46	VSS[182]	VSS[282]	M46
BC14	VSS[183]	VSS[283]	M8
BC18	VSS[184]	VSS[284]	N47
BC22	VSS[185]	VSS[285]	N48
BC26	VSS[186]	VSS[286]	P11
BC32	VSS[187]	VSS[287]	P18
BC34	VSS[188]	VSS[288]	T33
BC36	VSS[189]	VSS[289]	P40
BC40	VSS[190]	VSS[290]	P42
BC42	VSS[191]	VSS[291]	P43
BC48	VSS[192]	VSS[292]	P47
D46	VSS[193]	VSS[293]	P7
BD5	VSS[194]	VSS[294]	R2
BE22	VSS[195]	VSS[295]	R48
BE26	VSS[196]	VSS[296]	T12
BE40	VSS[197]	VSS[297]	T31
BE10	VSS[198]	VSS[298]	T37
BE12	VSS[199]	VSS[299]	T4
BE16	VSS[200]	VSS[300]	W34
BE20	VSS[201]	VSS[301]	W46
BE24	VSS[202]	VSS[302]	T47
BE28	VSS[203]	VSS[303]	T8
BE30	VSS[204]	VSS[304]	V11
BE38	VSS[205]	VSS[305]	V17
BF40	VSS[206]	VSS[306]	V26
BF8	VSS[207]	VSS[307]	V27
BF16	VSS[208]	VSS[308]	V29
BF20	VSS[209]	VSS[309]	V31
BF24	VSS[210]	VSS[310]	V36
BF28	VSS[211]	VSS[311]	V38
BF30	VSS[212]	VSS[312]	V43
BF38	VSS[213]	VSS[313]	V7
BF42	VSS[214]	VSS[314]	W17
BF44	VSS[215]	VSS[315]	W19
BF48	VSS[216]	VSS[316]	W2
BH11	VSS[217]	VSS[317]	W27
BH15	VSS[218]	VSS[318]	W48
BH17	VSS[219]	VSS[319]	Y12
BH19	VSS[220]	VSS[320]	Y38
BH27	VSS[221]	VSS[321]	Y4
BH31	VSS[222]	VSS[322]	Y42
BH33	VSS[223]	VSS[323]	Y46
BH35	VSS[224]	VSS[324]	Y8
BH43	VSS[225]	VSS[325]	BG29
BH7	VSS[226]	VSS[326]	N24
D3	VSS[227]	VSS[327]	AJ3
D12	VSS[228]	VSS[328]	AD47
D16	VSS[229]	VSS[329]	B43
D18	VSS[230]	VSS[330]	BE10
D22	VSS[231]	VSS[331]	BG41
D24	VSS[232]	VSS[332]	G14
D26	VSS[233]	VSS[333]	H16
D28	VSS[234]	VSS[334]	H36
D30	VSS[235]	VSS[335]	BG22
D32	VSS[236]	VSS[336]	BG24
D34	VSS[237]	VSS[337]	BG24
D38	VSS[238]	VSS[338]	C22
D42	VSS[239]	VSS[339]	AP13
D8	VSS[240]	VSS[340]	M14
E18	VSS[241]	VSS[341]	AP3
E26	VSS[242]	VSS[342]	AP1
G18	VSS[243]	VSS[343]	BE16
G20	VSS[244]	VSS[344]	BC16
G26	VSS[245]	VSS[345]	BC28
G28	VSS[246]	VSS[346]	BJ28
G36	VSS[247]	VSS[347]	
G48	VSS[248]	VSS[348]	
H12	VSS[249]	VSS[349]	
H18	VSS[250]	VSS[350]	
H22	VSS[251]	VSS[351]	
H24	VSS[252]	VSS[352]	
H26	VSS[253]		
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H34	VSS[256]		
F3	VSS[257]		
	VSS[258]		

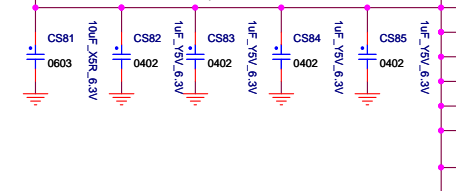
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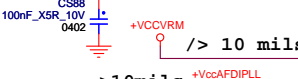
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+V1.05S\_VCCP 2925mA />240mils



+V3.3S 50mA />10mils



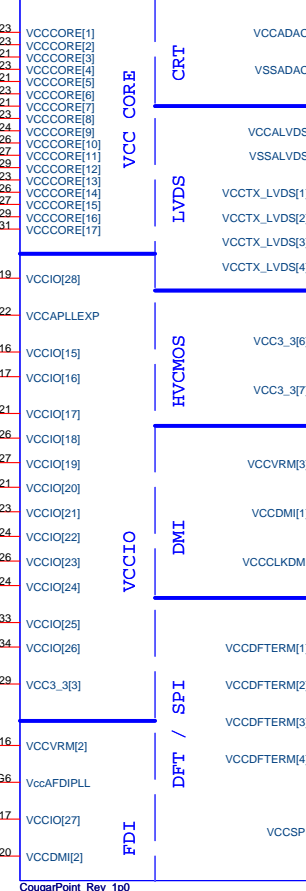
+V1.05S\_VCCP >10mils



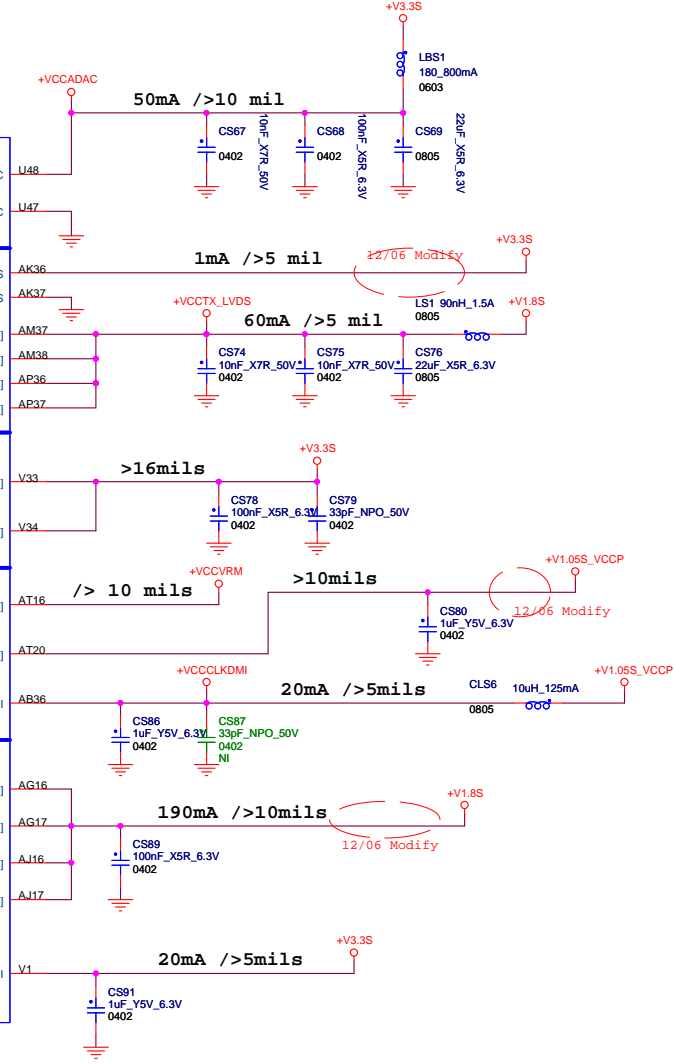
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## POWER

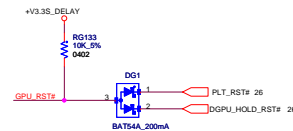
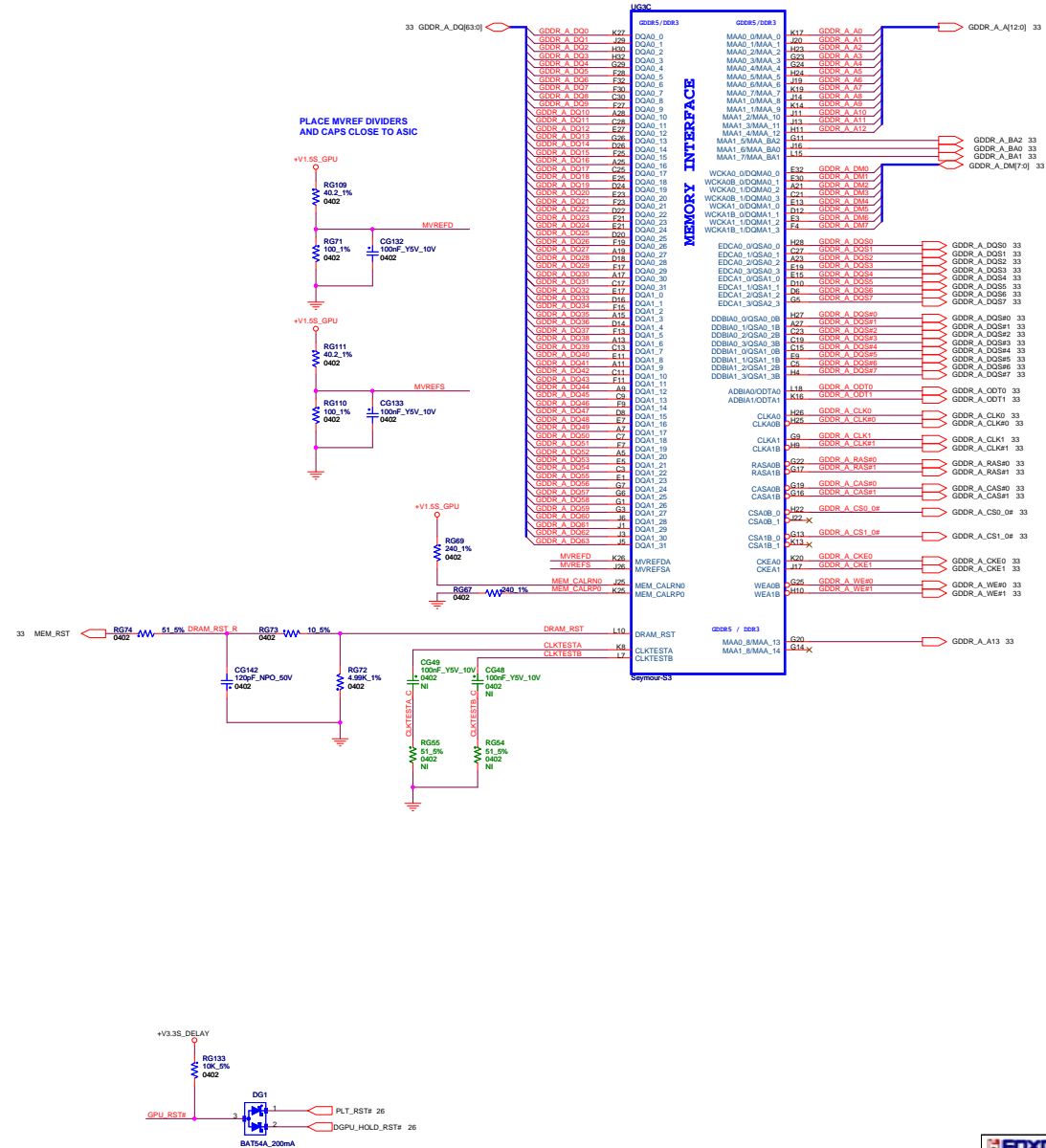
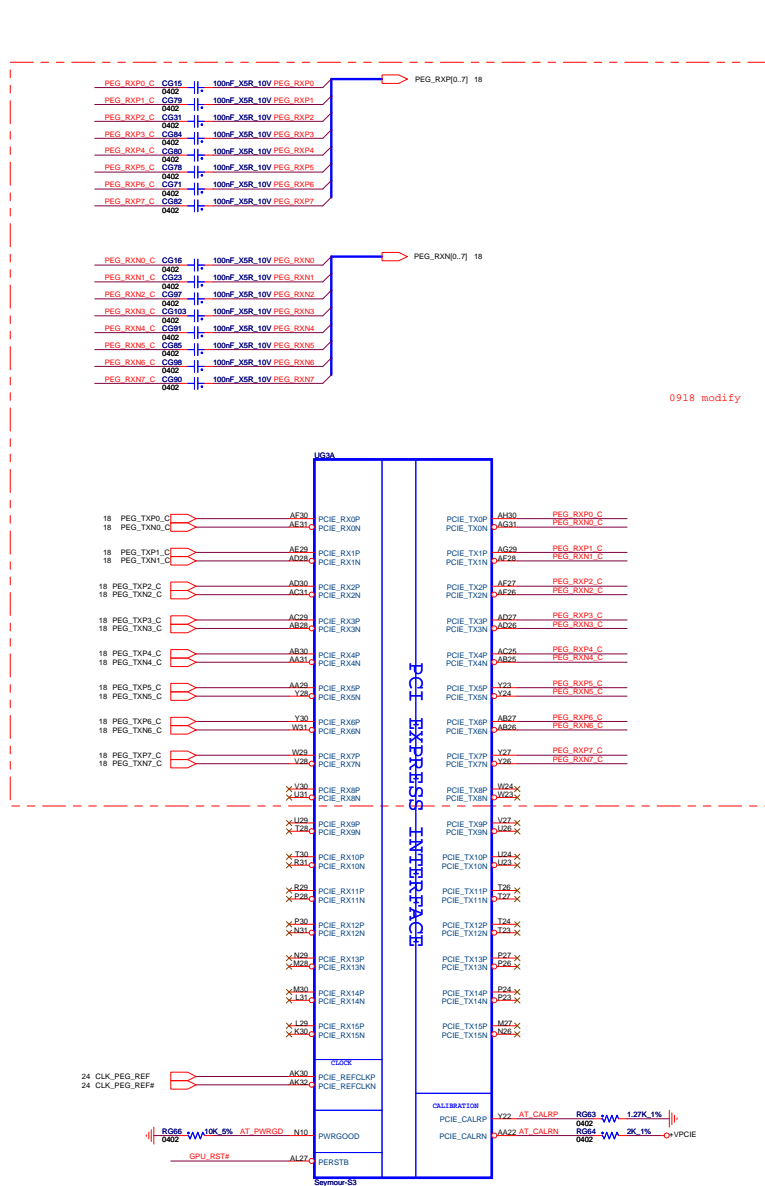


CougarPoint\_Rev\_1p0











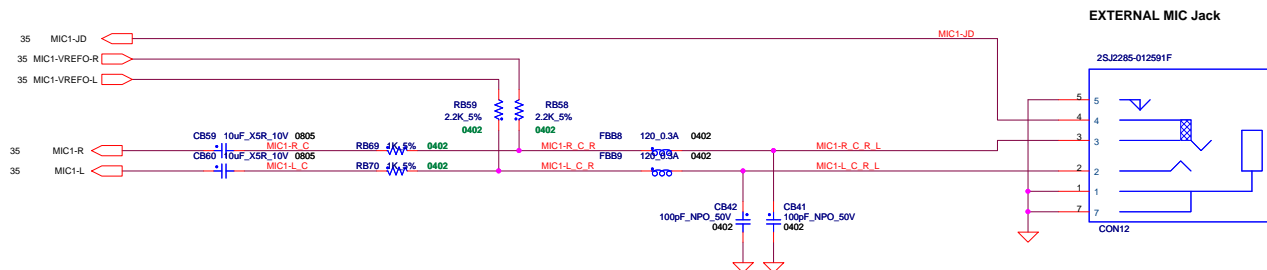
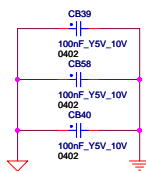
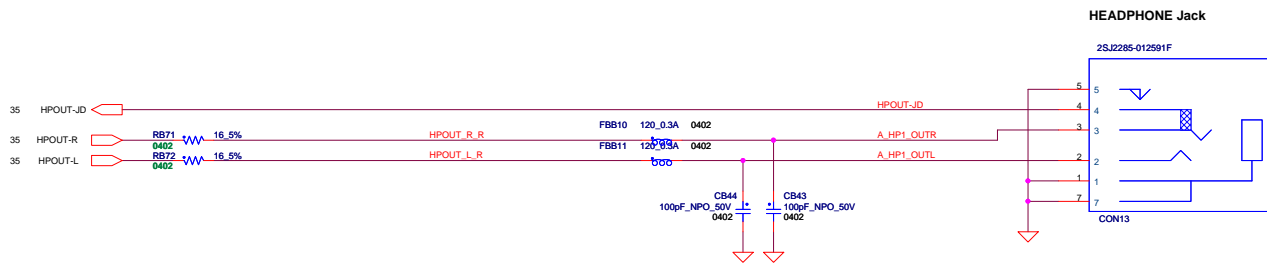
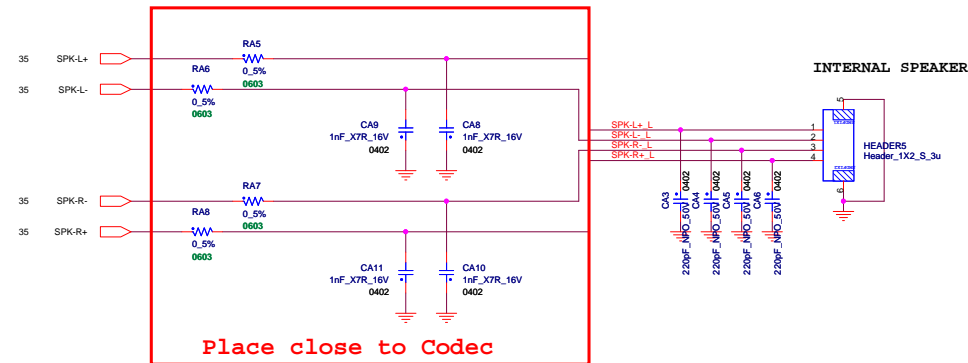
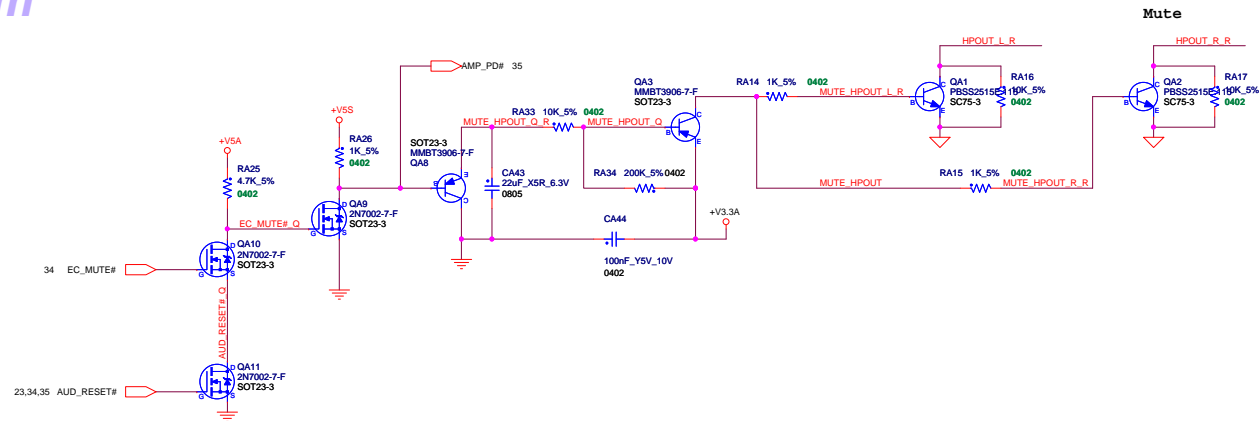


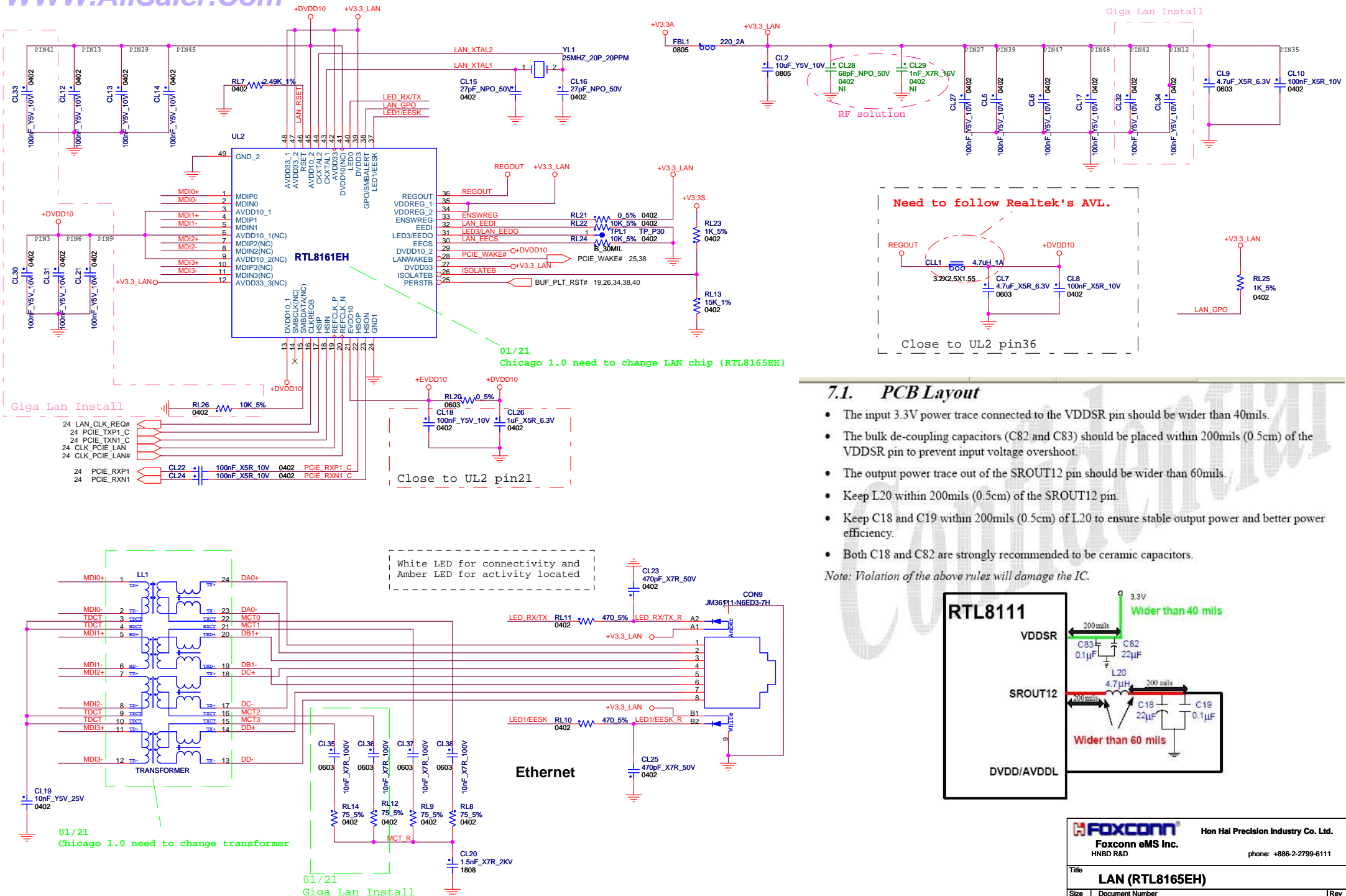


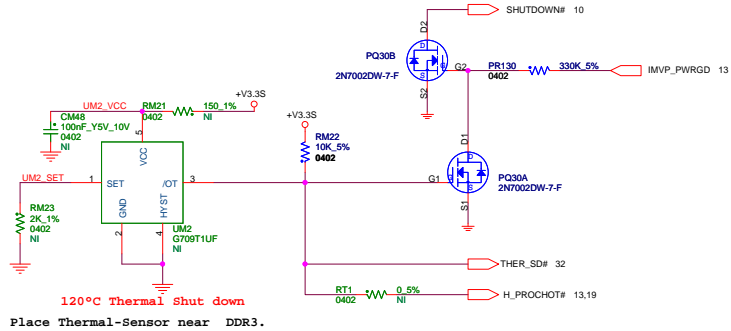
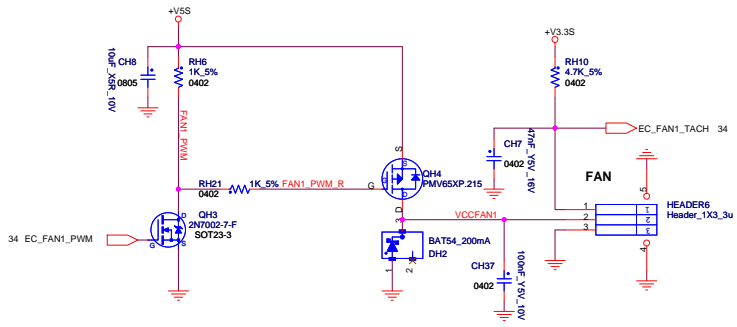
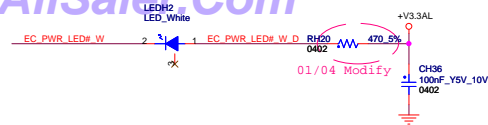




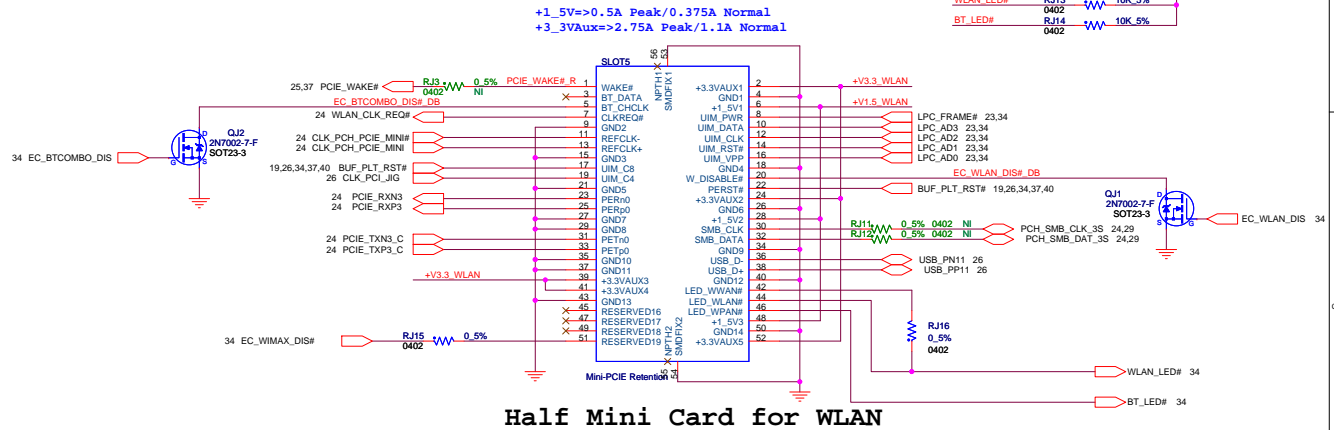
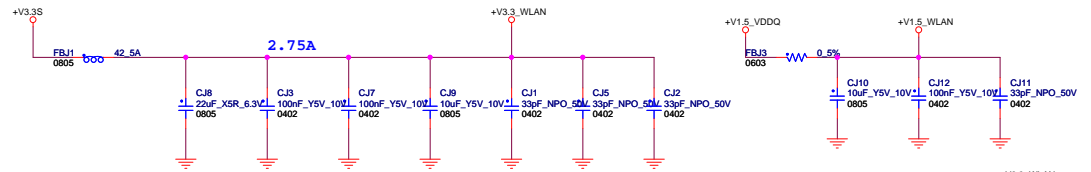
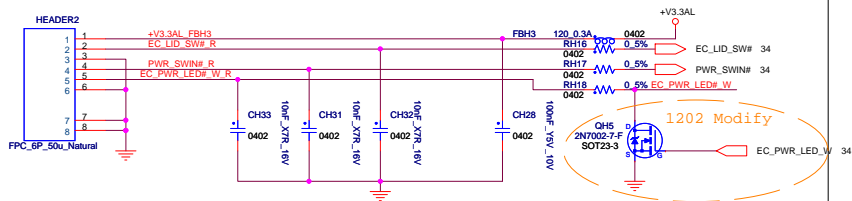




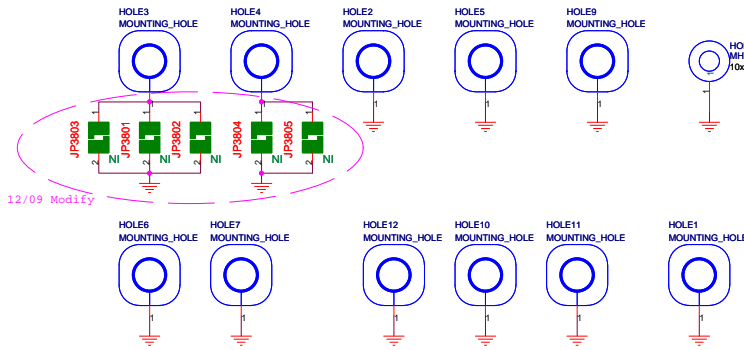




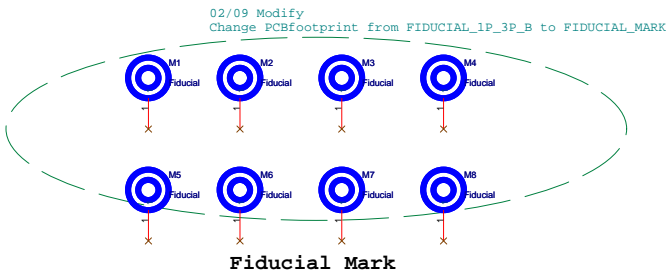
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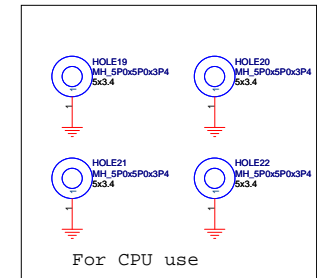
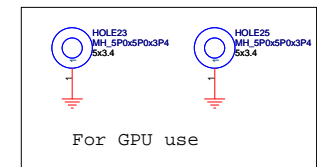
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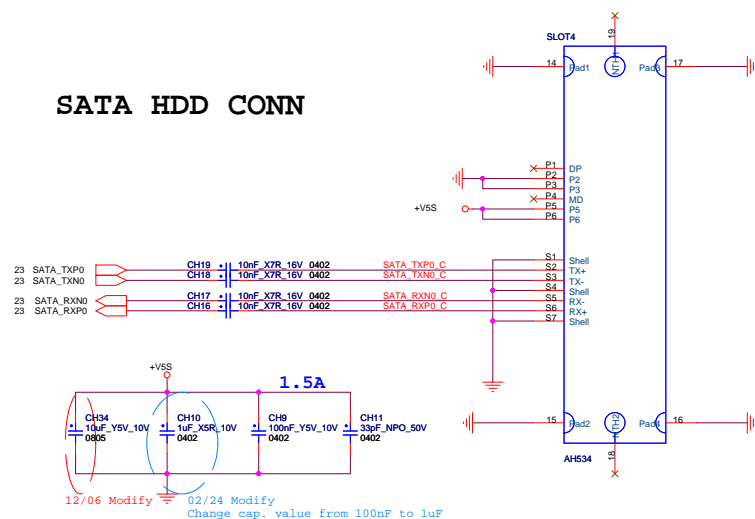
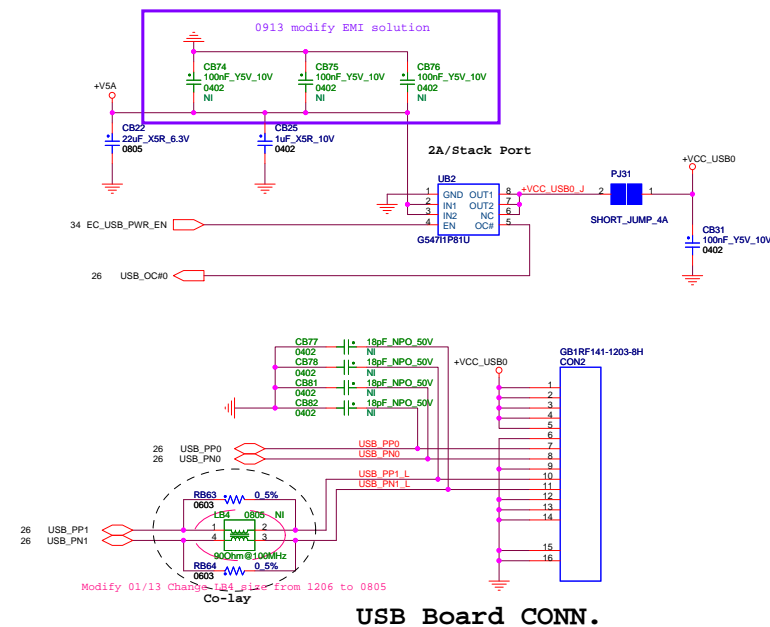
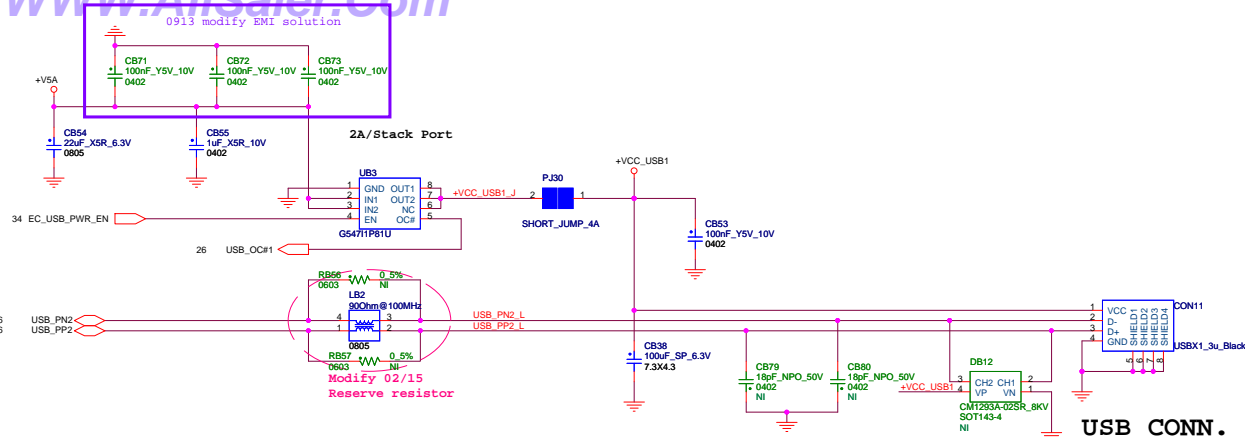


## Mounting HOLE

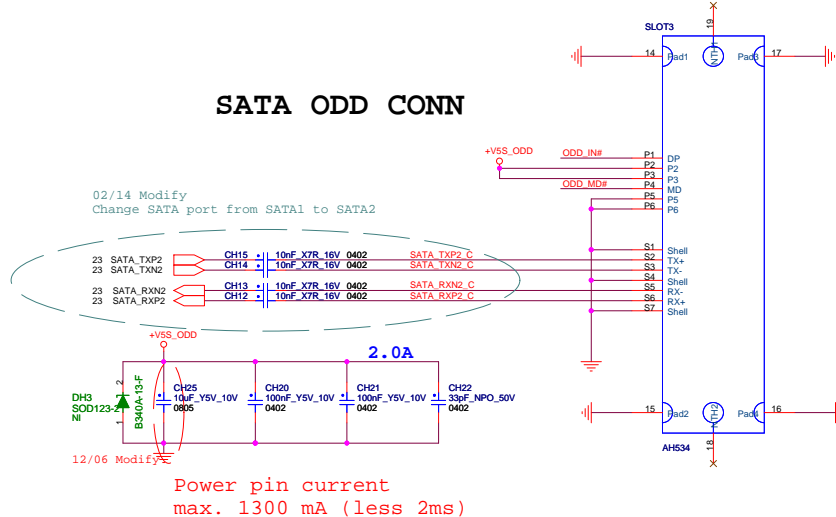


## Fiducial Mark

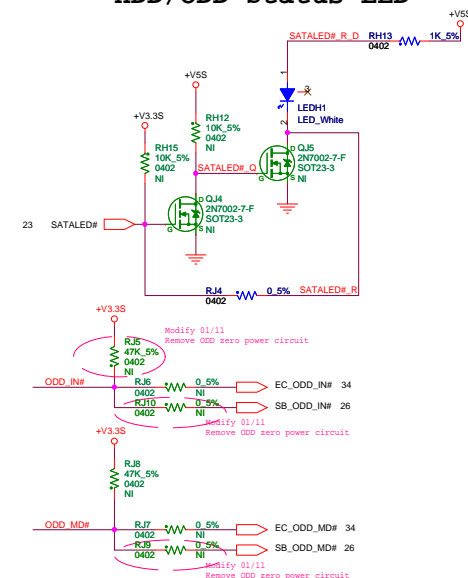




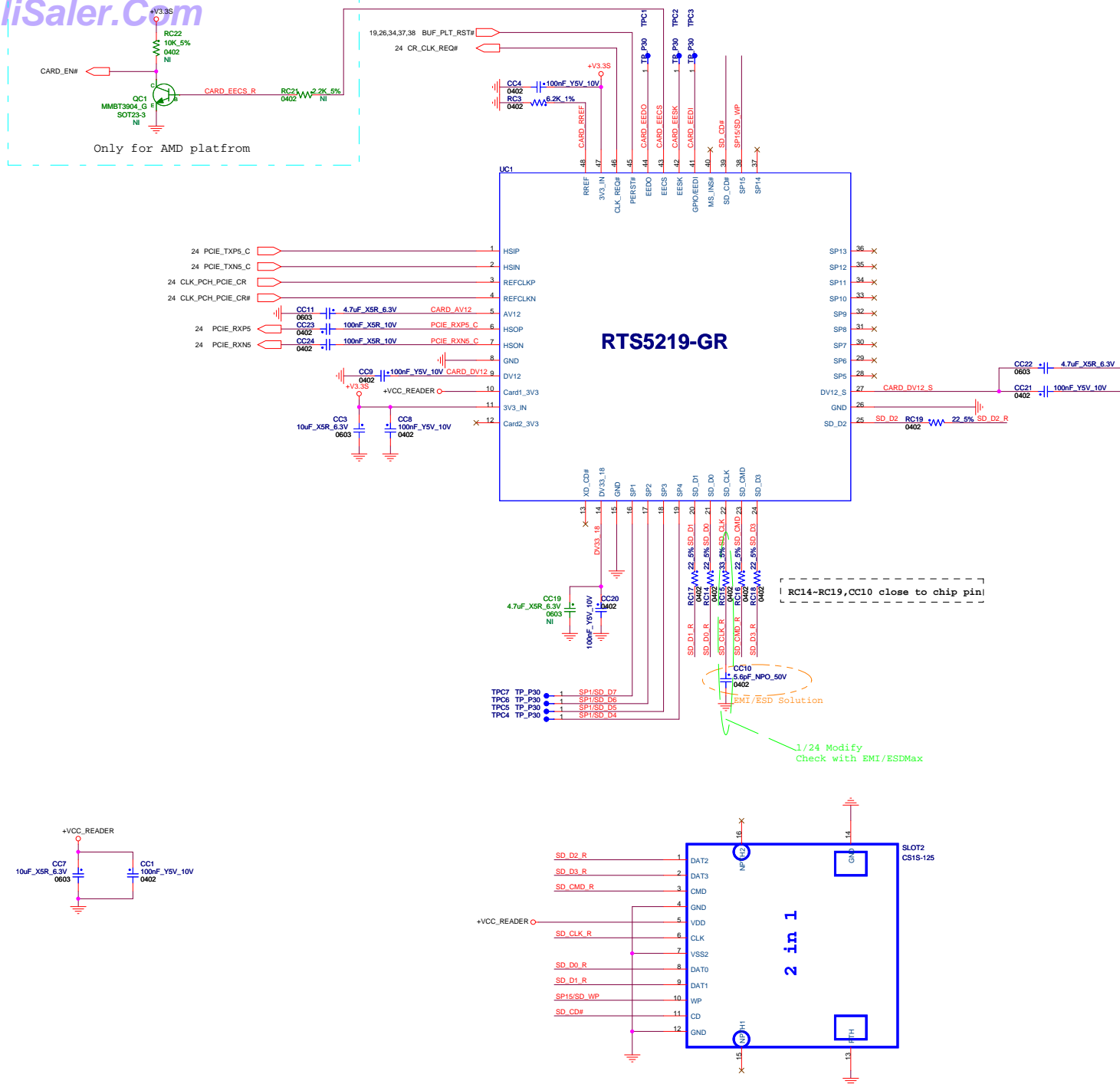
## SATA ODD CONN



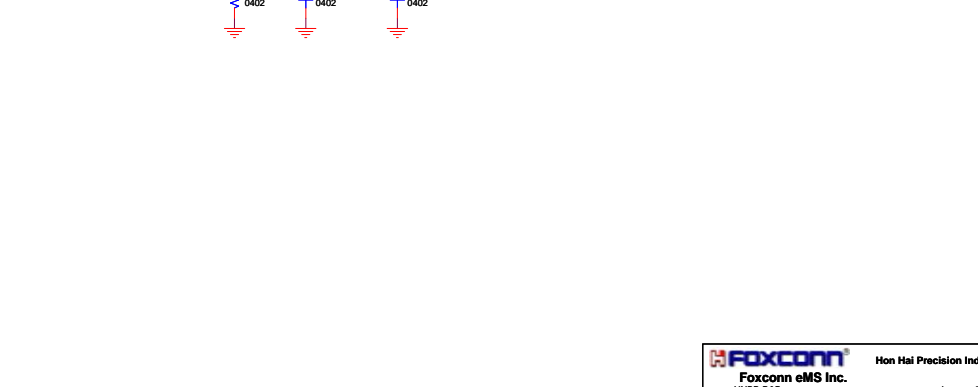
## HDD/ODD Status LED

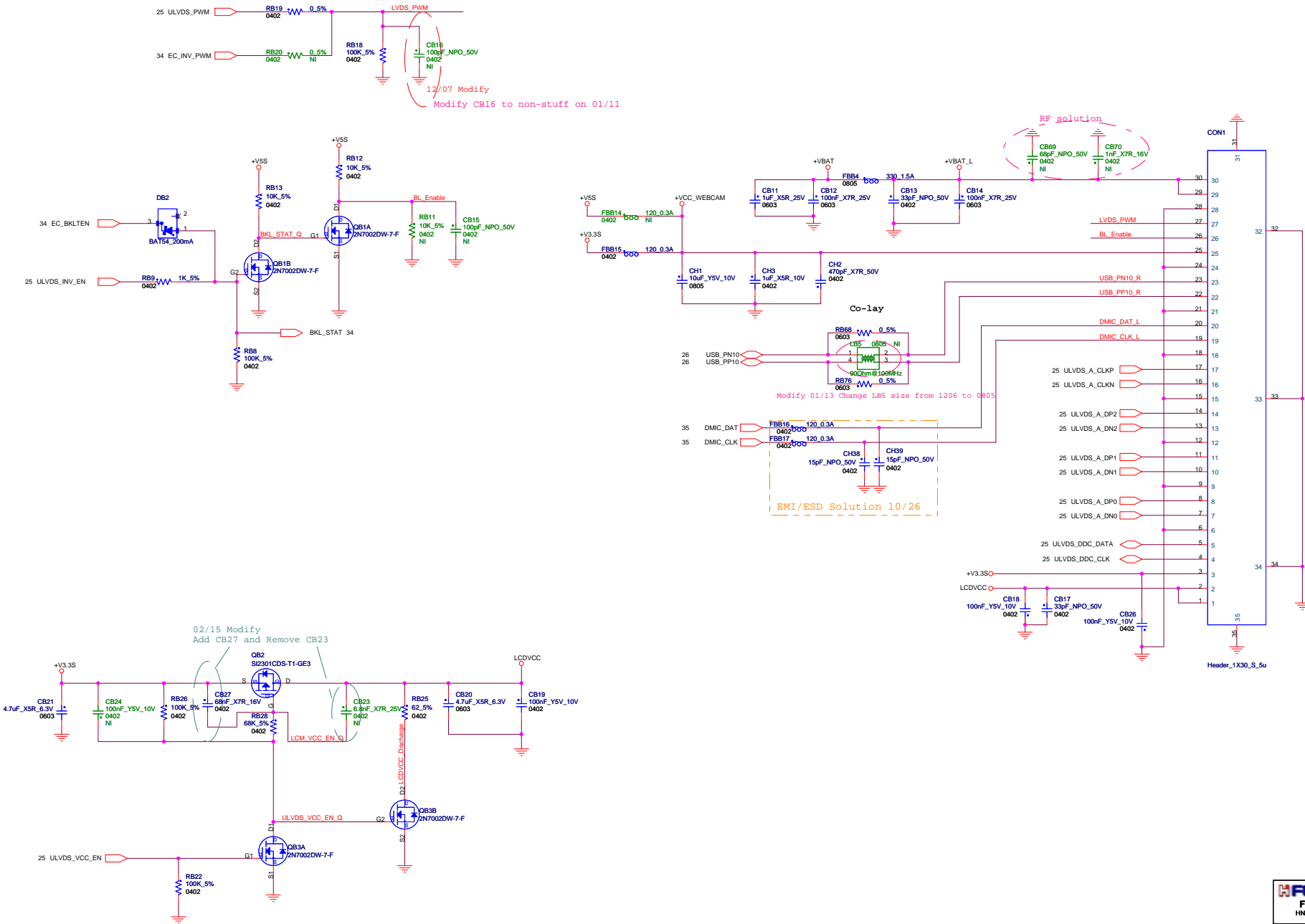


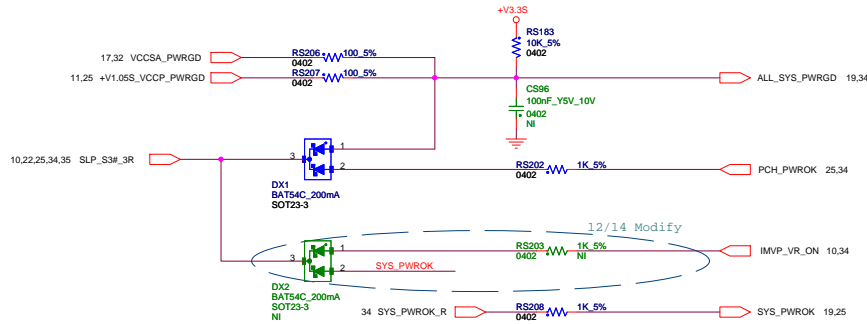




CRT



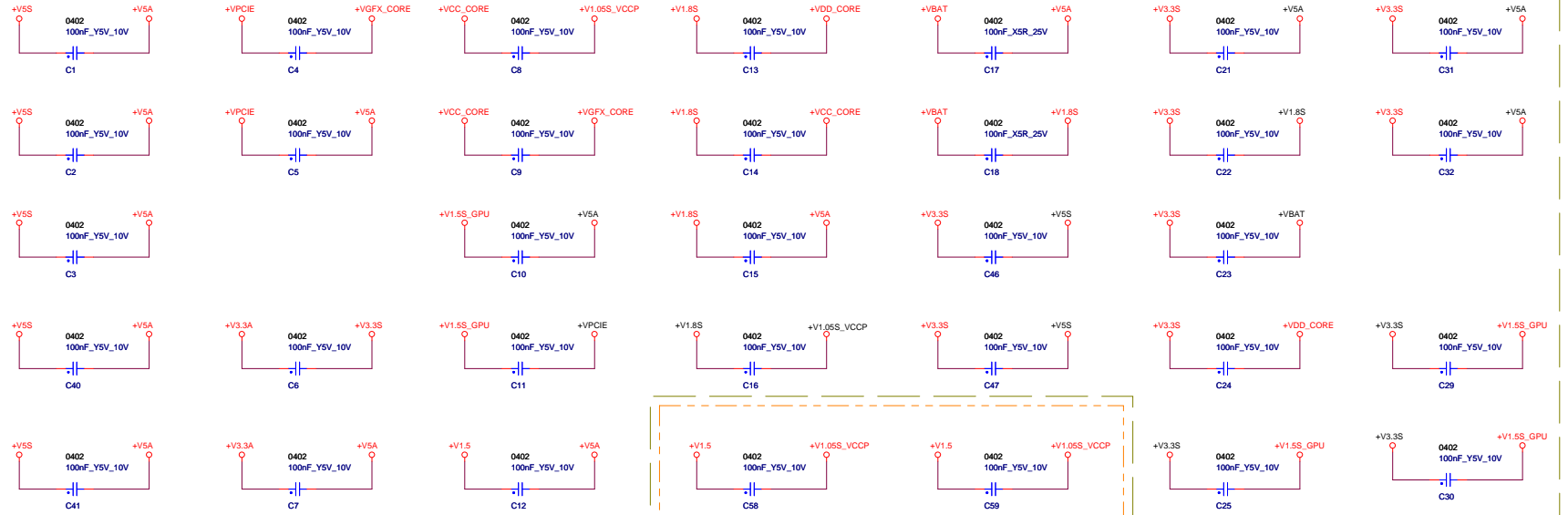
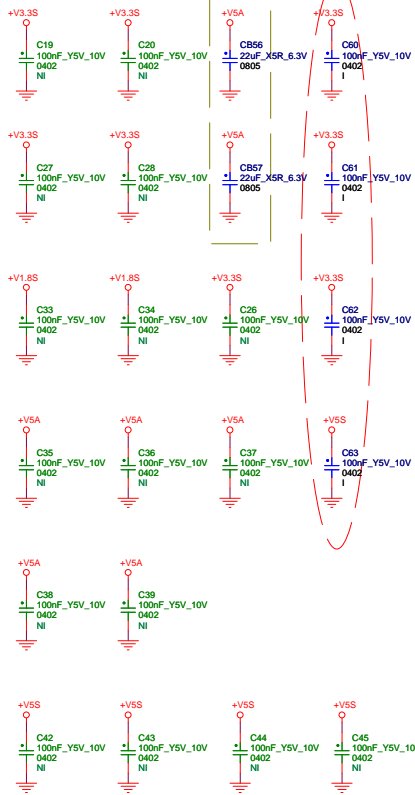




+V5S 12,14,23,27,32,35,36,38,39,41,42  
 +V3.3S 13,14,18,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42  
 +V3.3S\_DELAY 14,30,31,32

12/07 Modify  
 1117 Modify

Modify 11/11



EMI/ESD Solution 10/26

